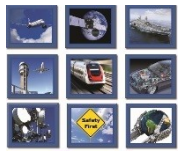




# Introduction to Nucleo-64 platform





- Intecs - Italian company with activities in:
  - Defense
  - Railway
  - Aerospace
  - Traffic Control & Surveillance
  - Automotive
  - Telecom
- Approx. 500 employees over 6 cities in Italy (not only)
- Purpose of these classes: getting familiar with the world of embedded systems and microcontrollers.

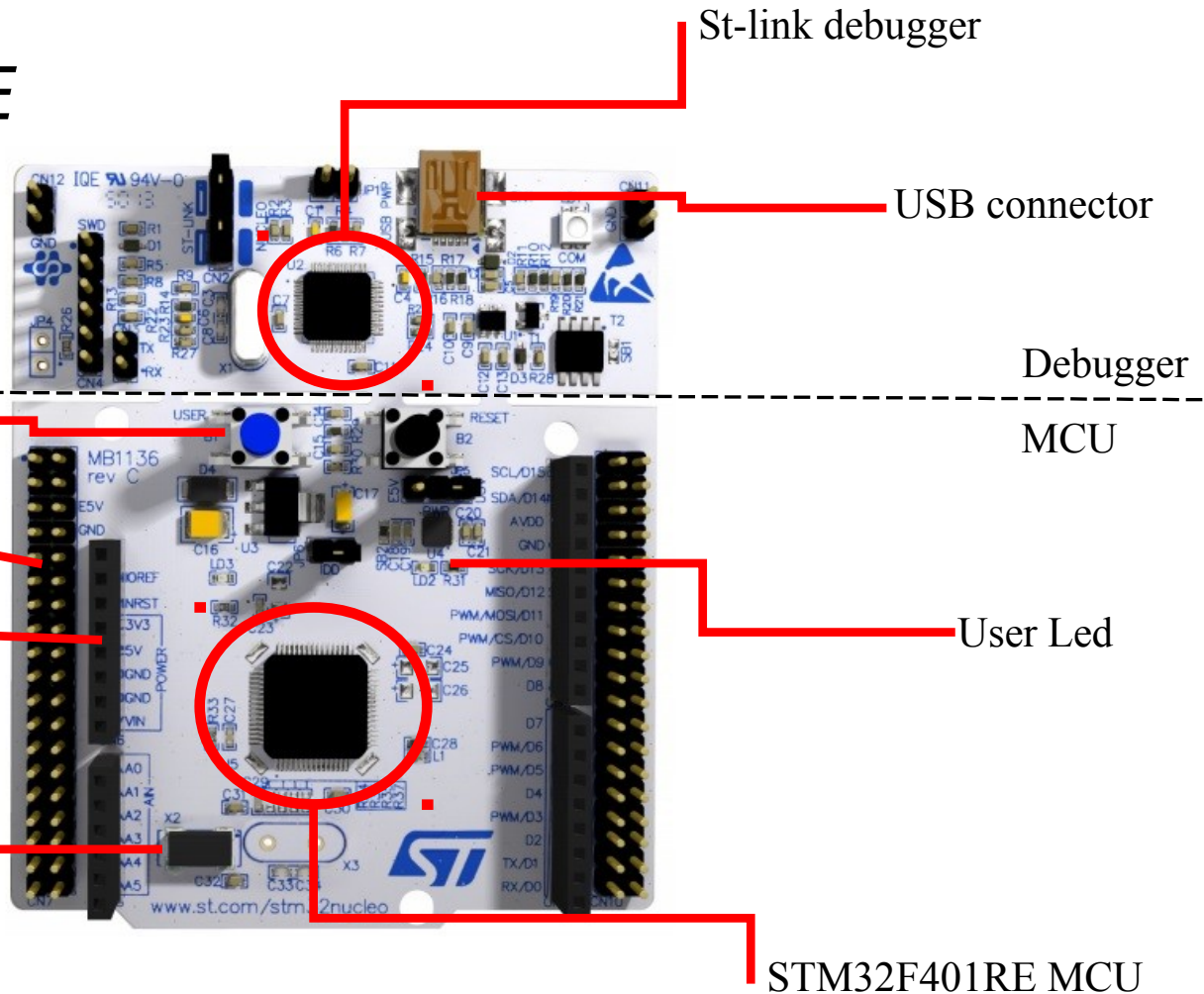
# Introducing myself



- PhD in computer engineering @diag
- Focus on wireless sensor networks and low power devices.
- Since 2012 partner of Wsense (university spin-off): hw + microcontroller software development.
- In Intecs since October 2016: head of HW Lab in Rome, embedded sw developer/hw designer.



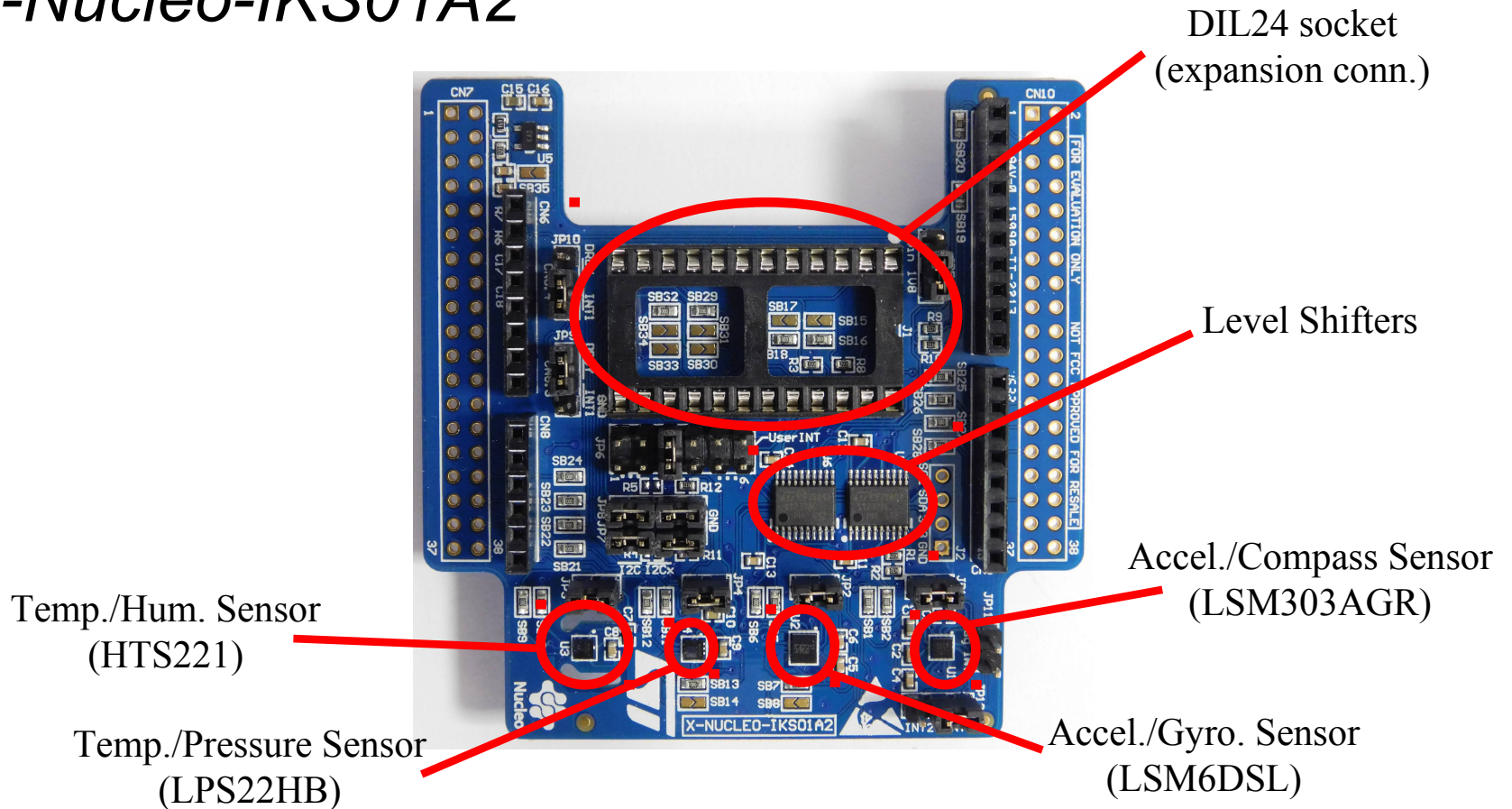
## The development board: *Nucleo-F401RE*



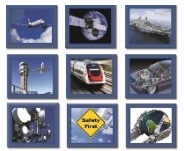


## Sensor expansion board:

### X-Nucleo-IKS01A2

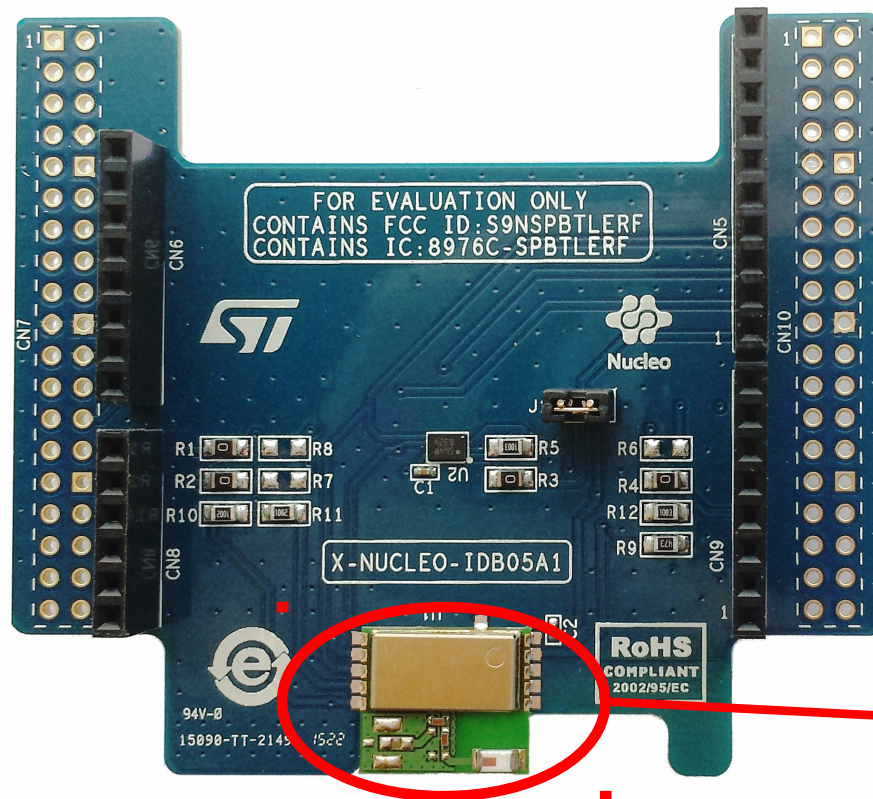






## Bluetooth expansion board:

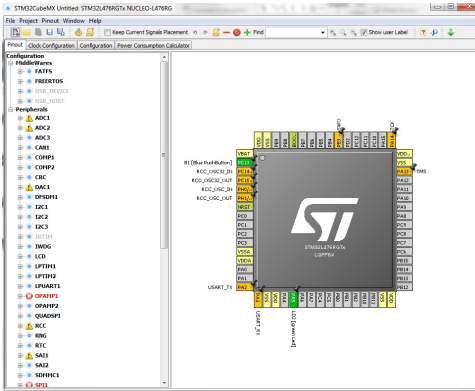
### X-Nucleo-IDB05A1



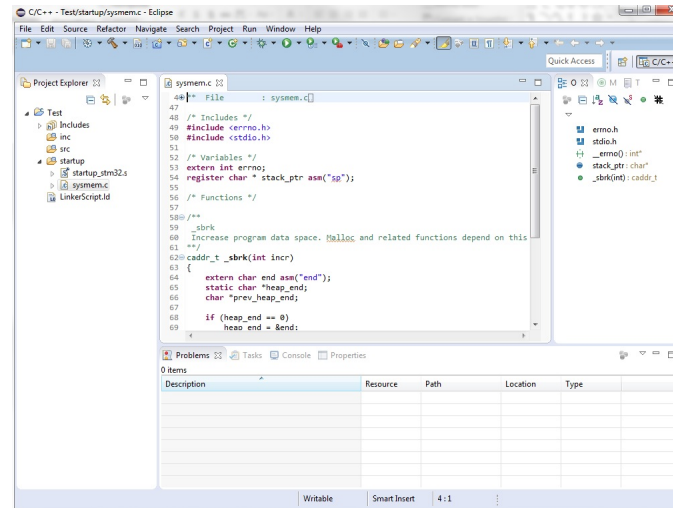
Bluetooth module (SPBTLE-RF)



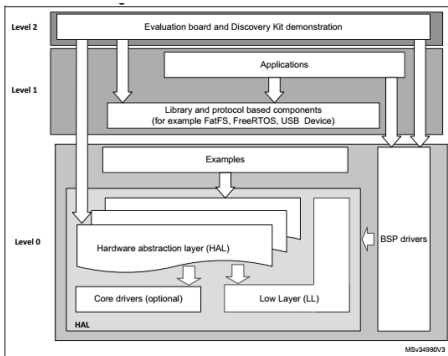
## Framework, IDE & tools



STM CubeMX

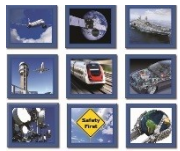


System Workbench 4



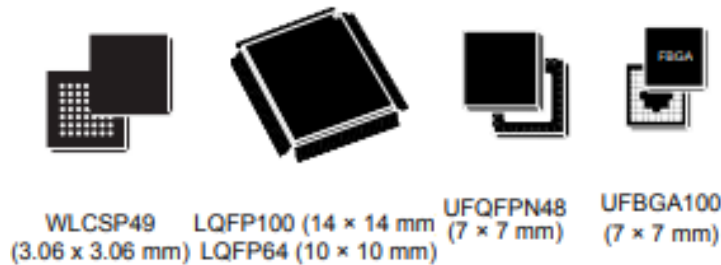
Stm32CubeF4

# The Microcontroller

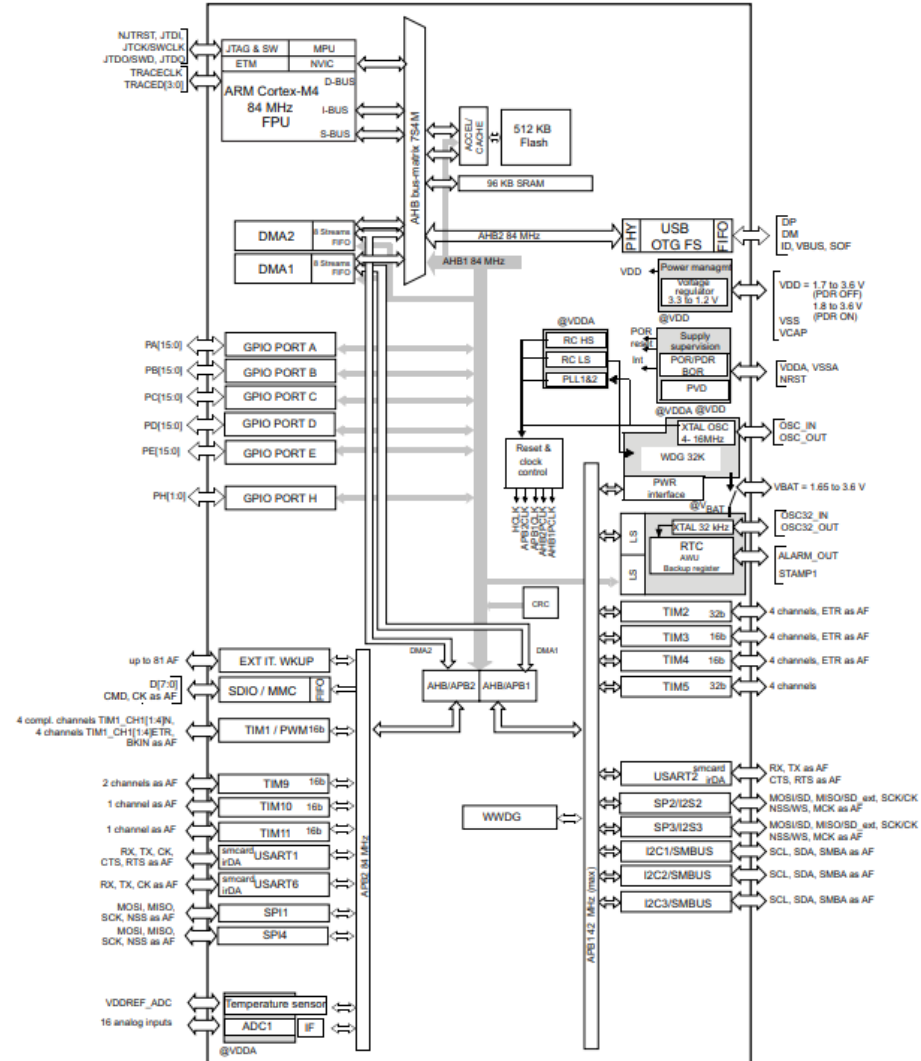


## Stm32F401 Microcontroller:

- Based on Cortex M4 processor
- 512KB ROM Flash memory
- 96KB SRAM data memory
- Up to 84Mhz operating frequency
- 42uA in sleep (stop mode) w/RTC

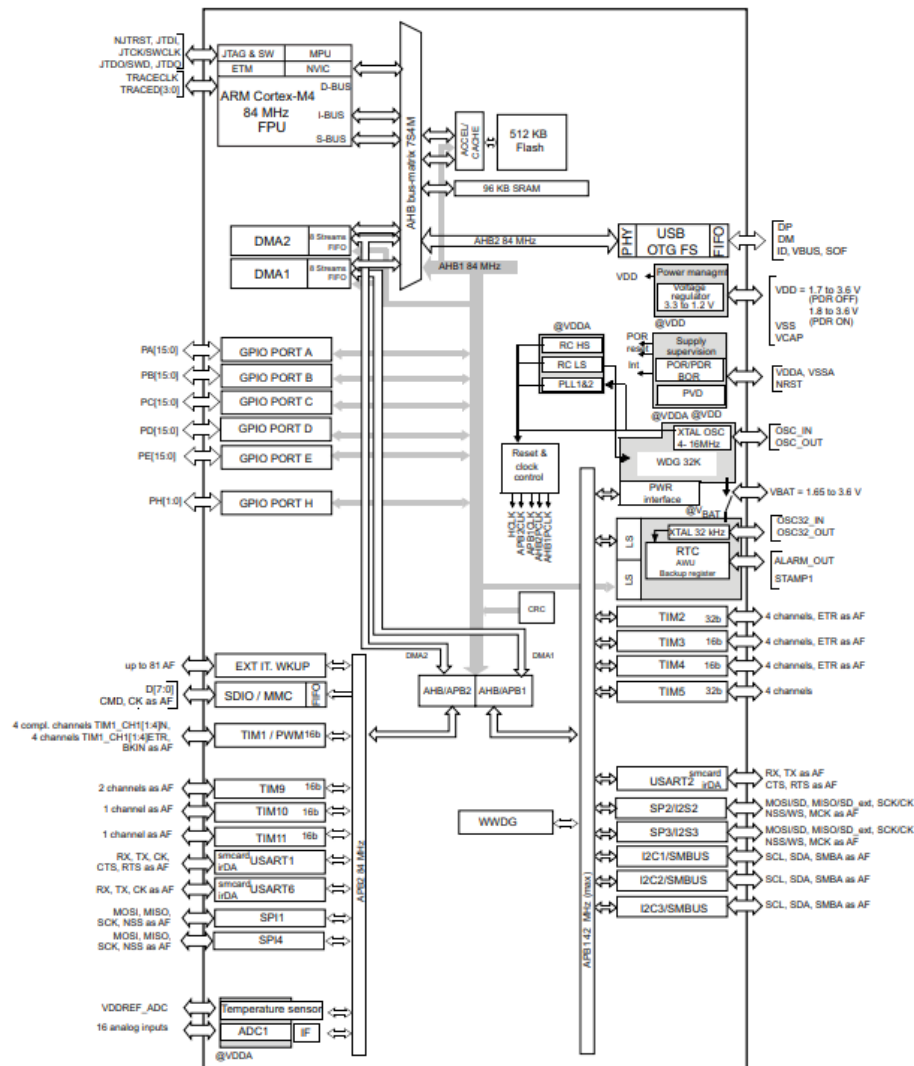
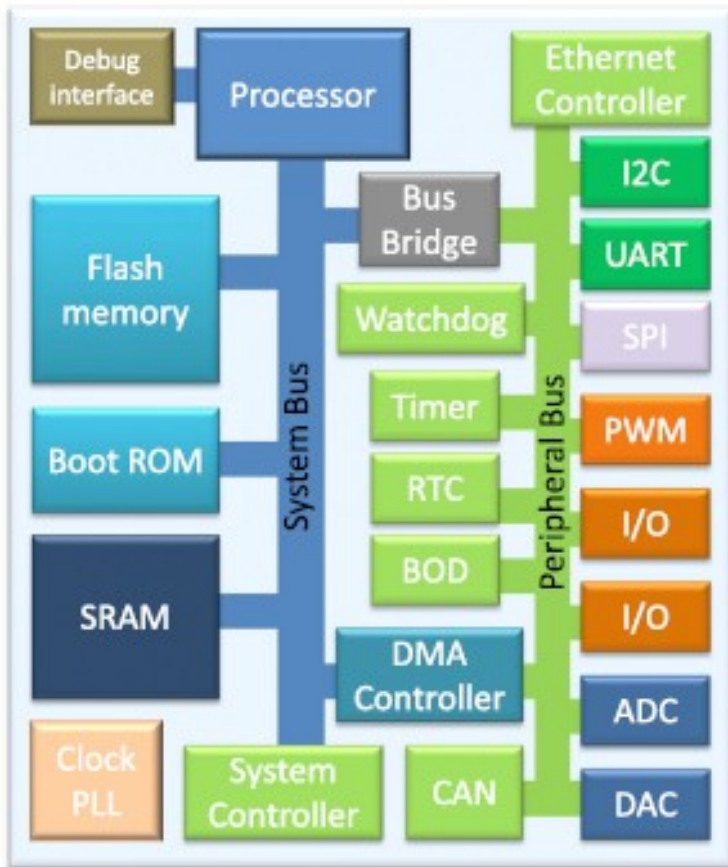
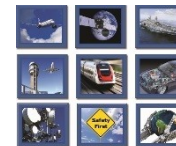


Available packages

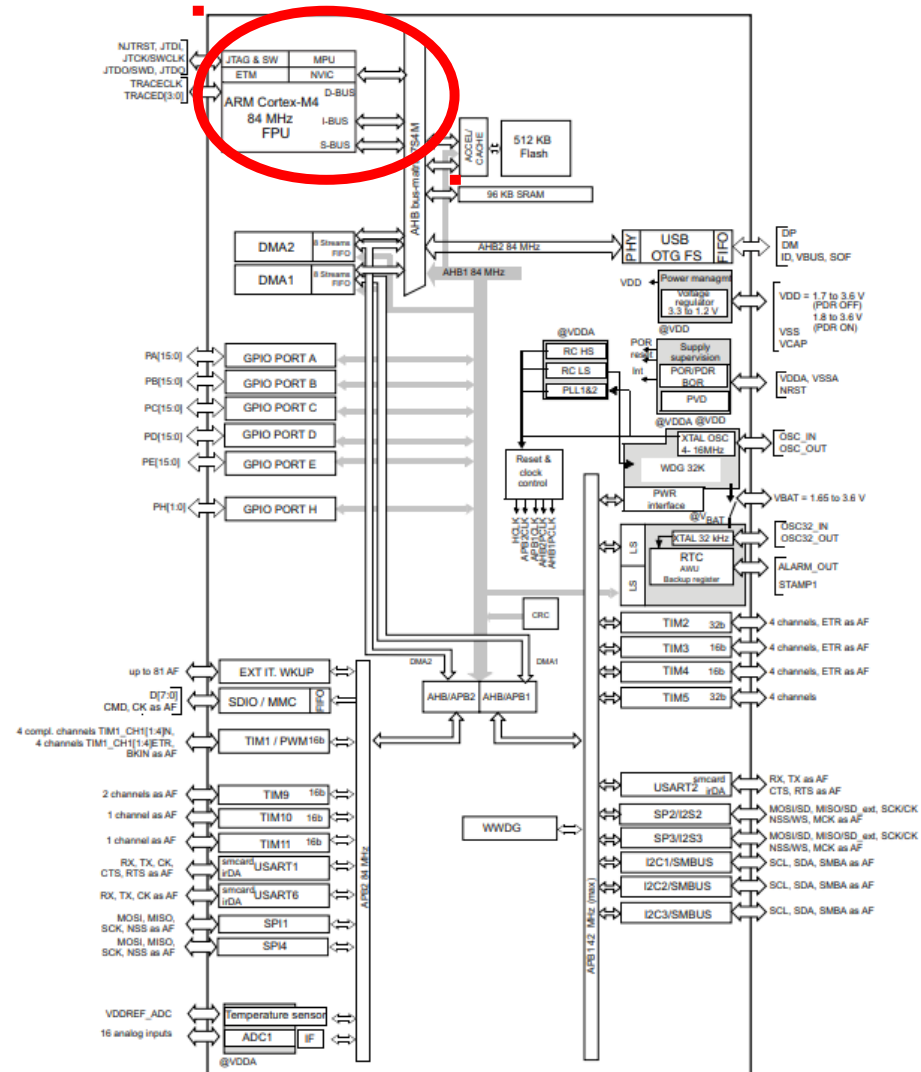
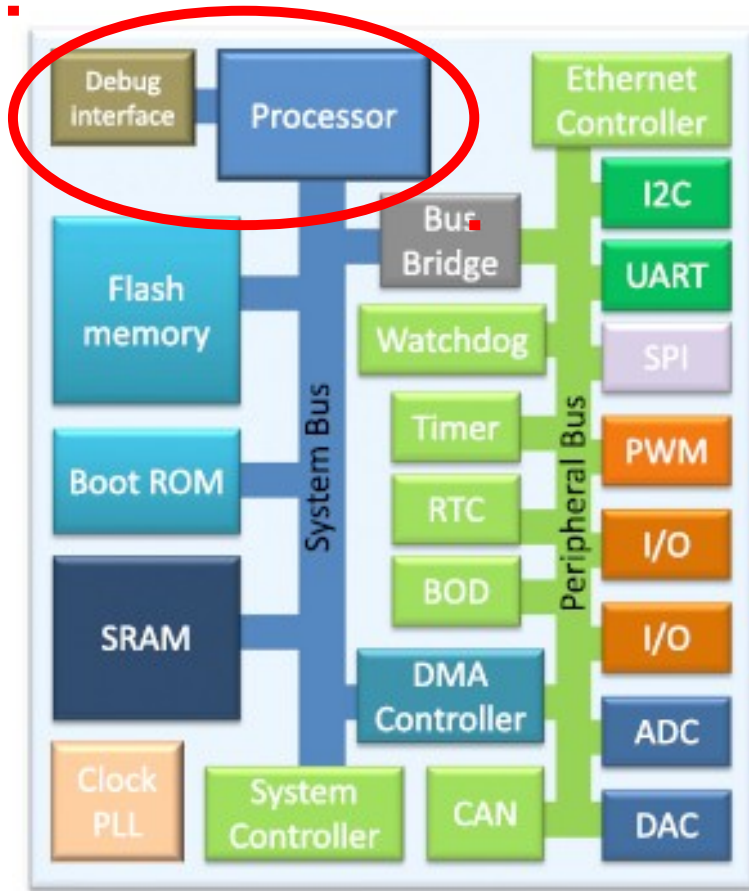




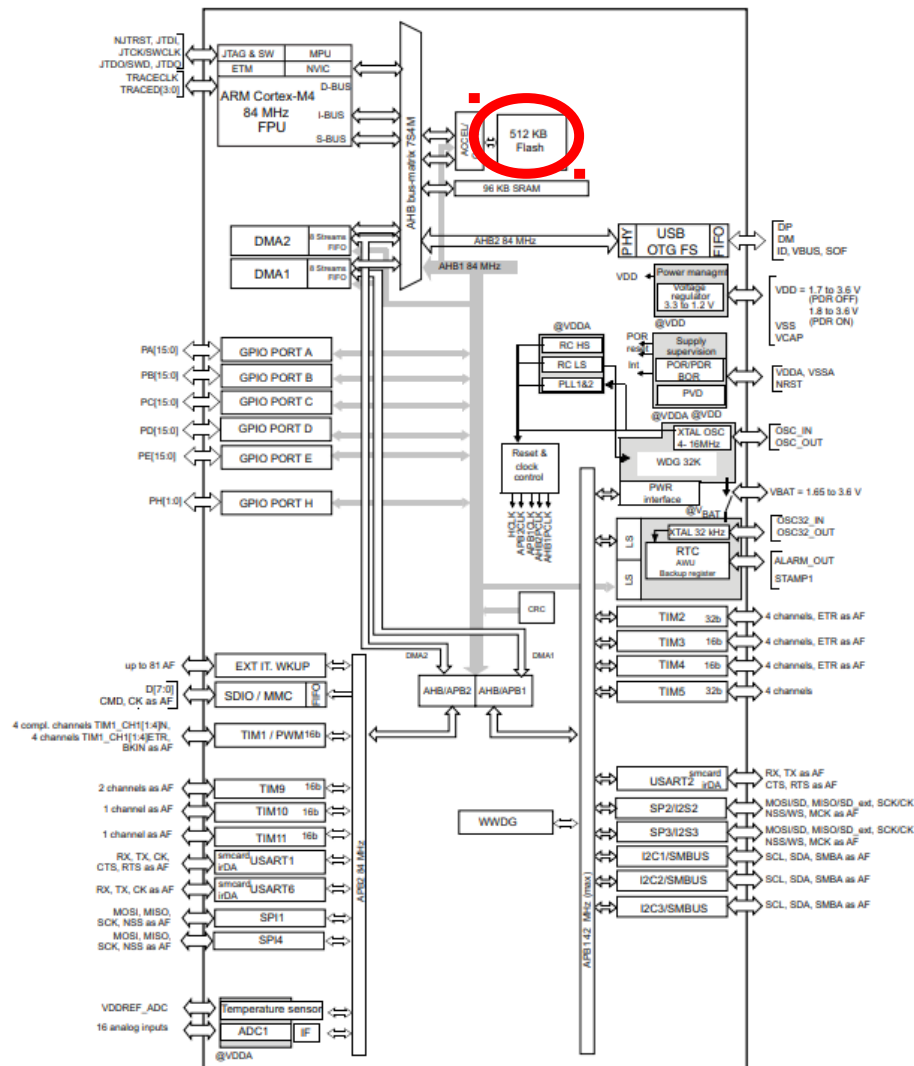
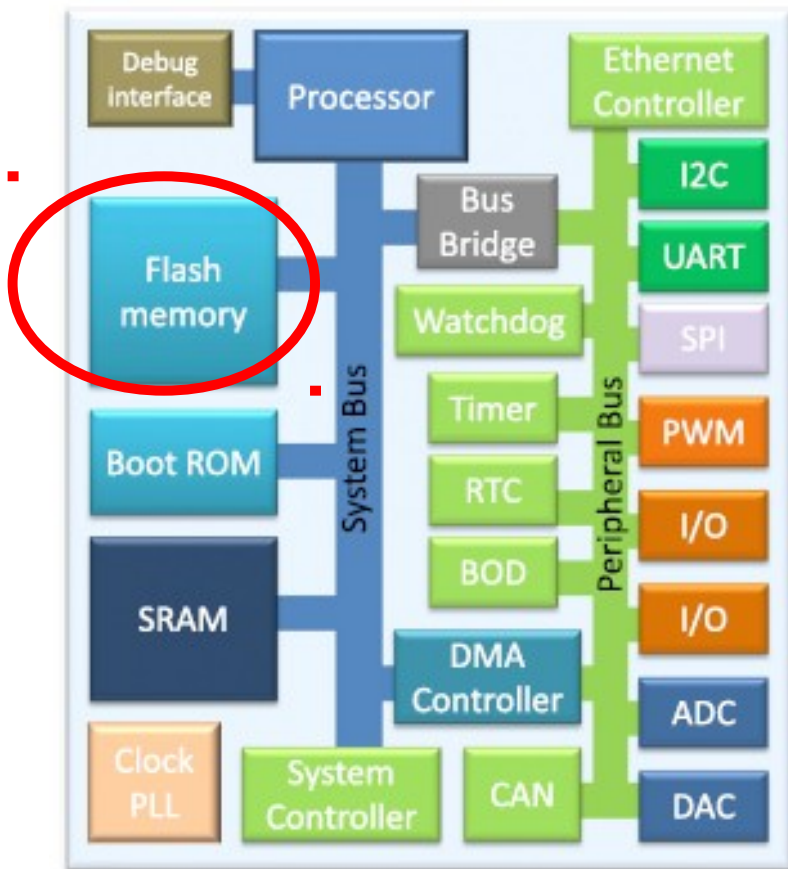
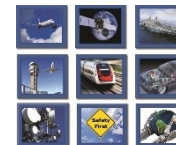
# Architecture



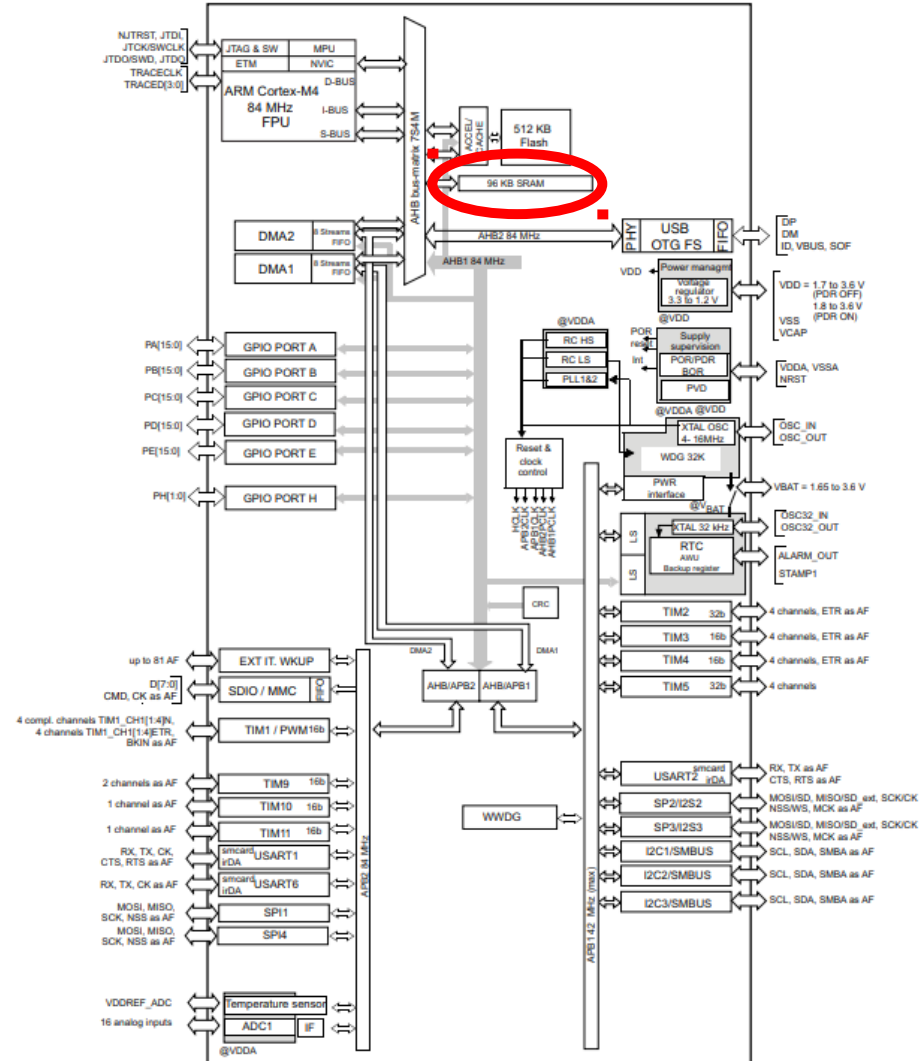
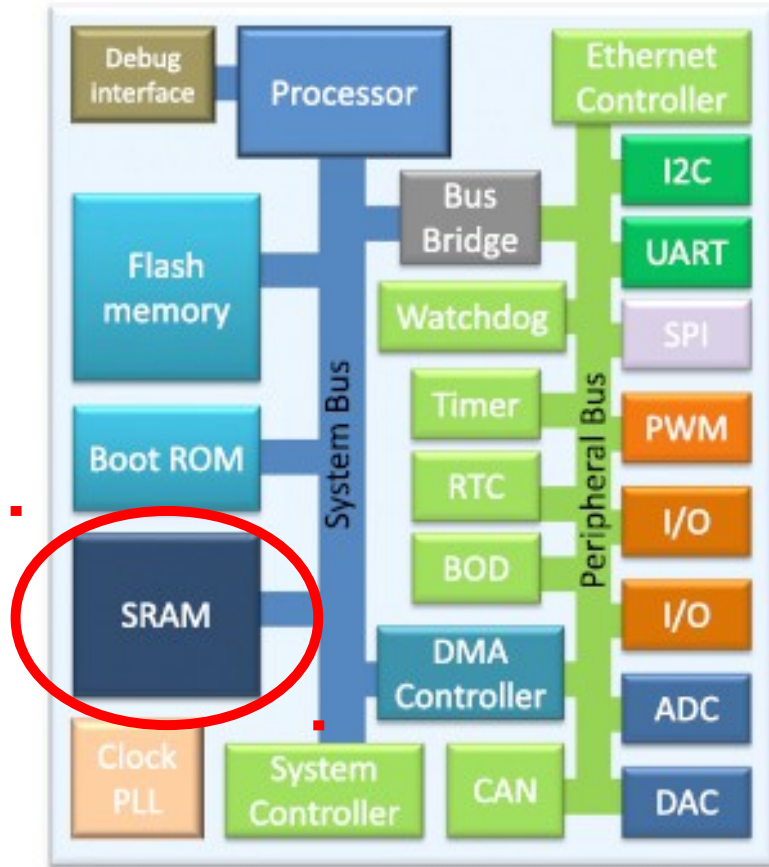
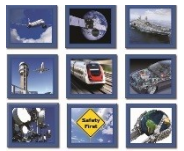
# Architecture



# Architecture

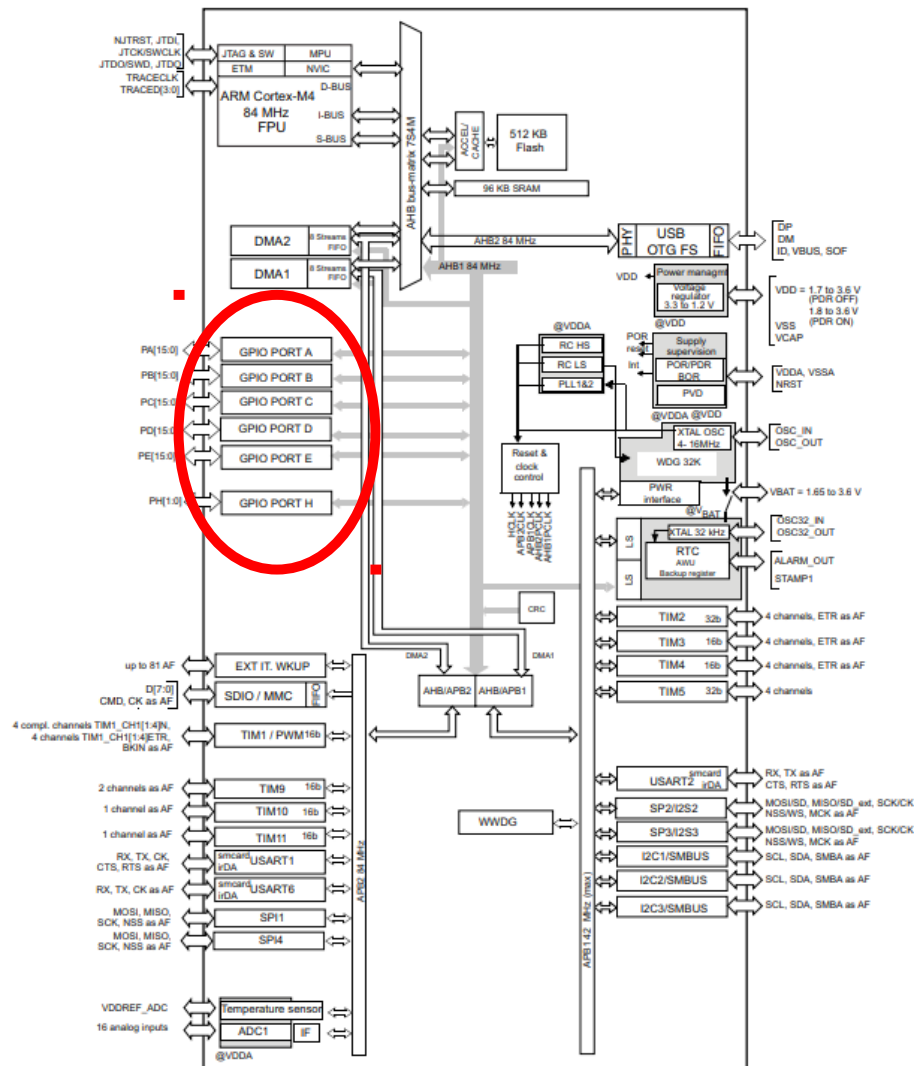
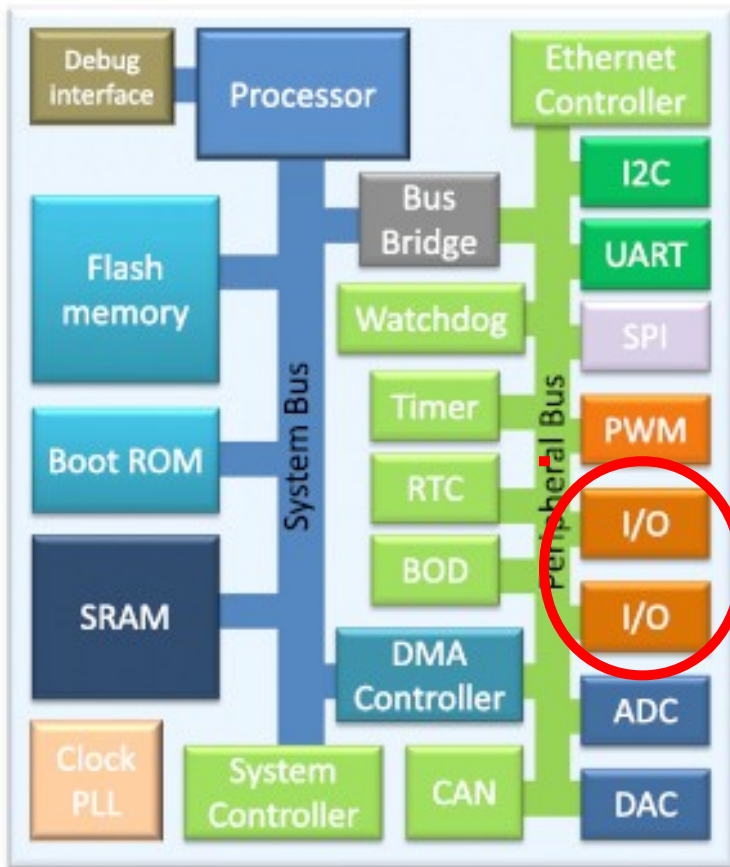
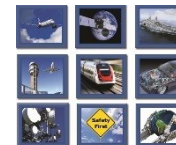


# Architecture



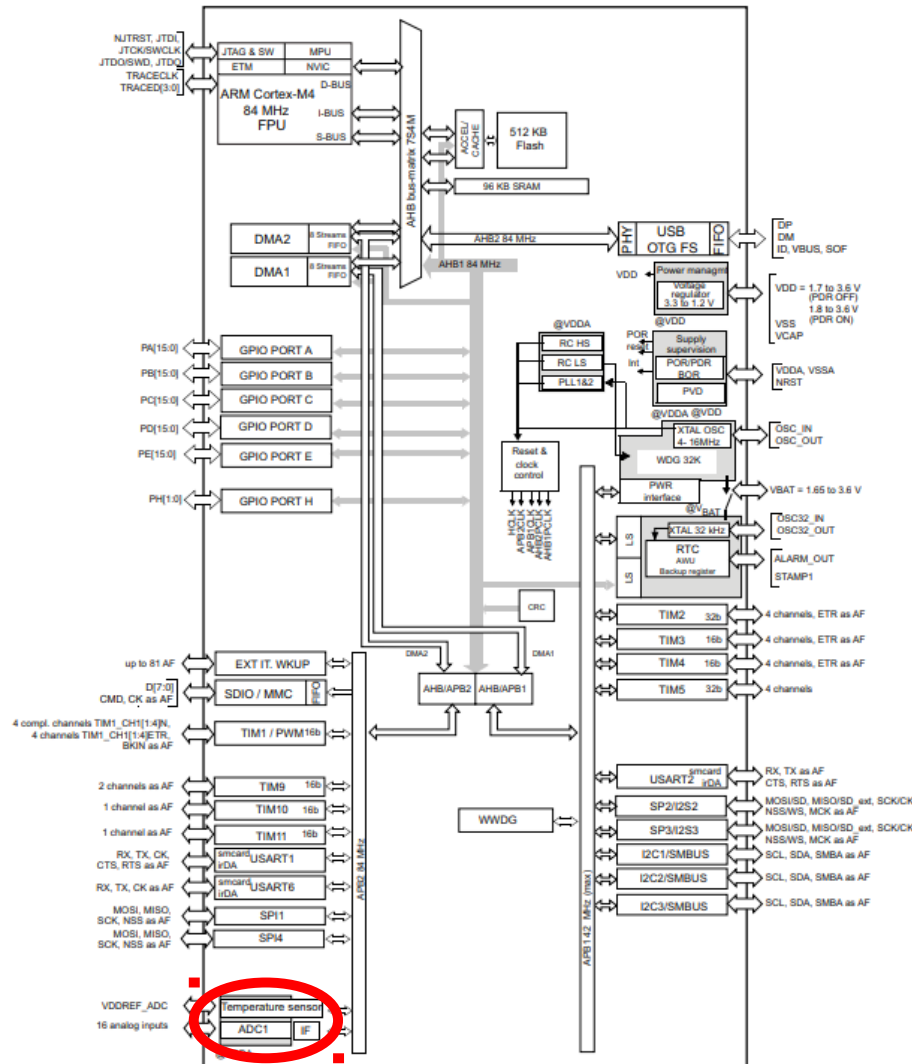
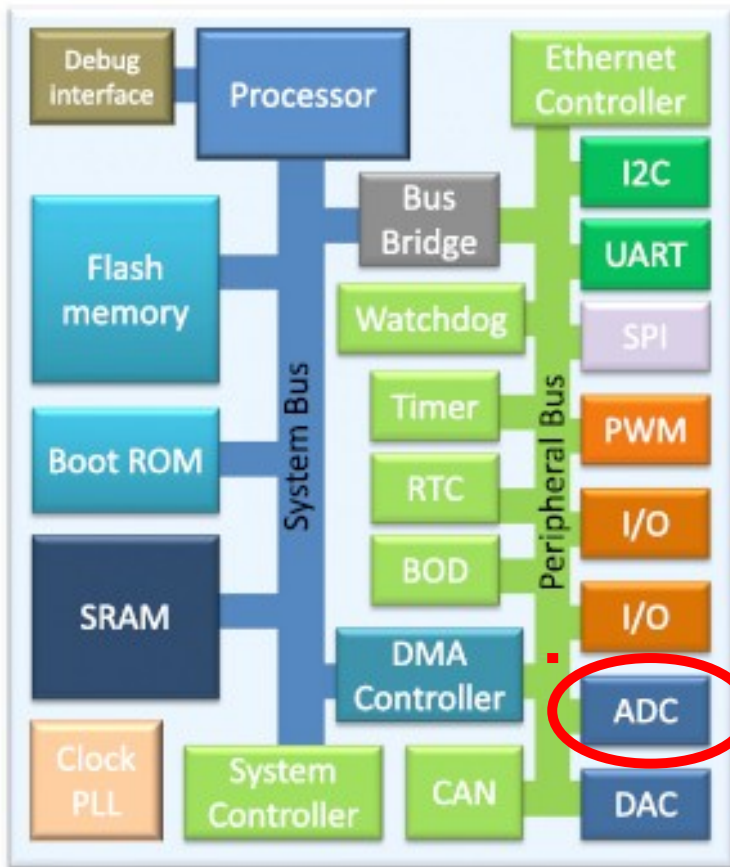
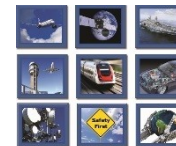


# Architecture

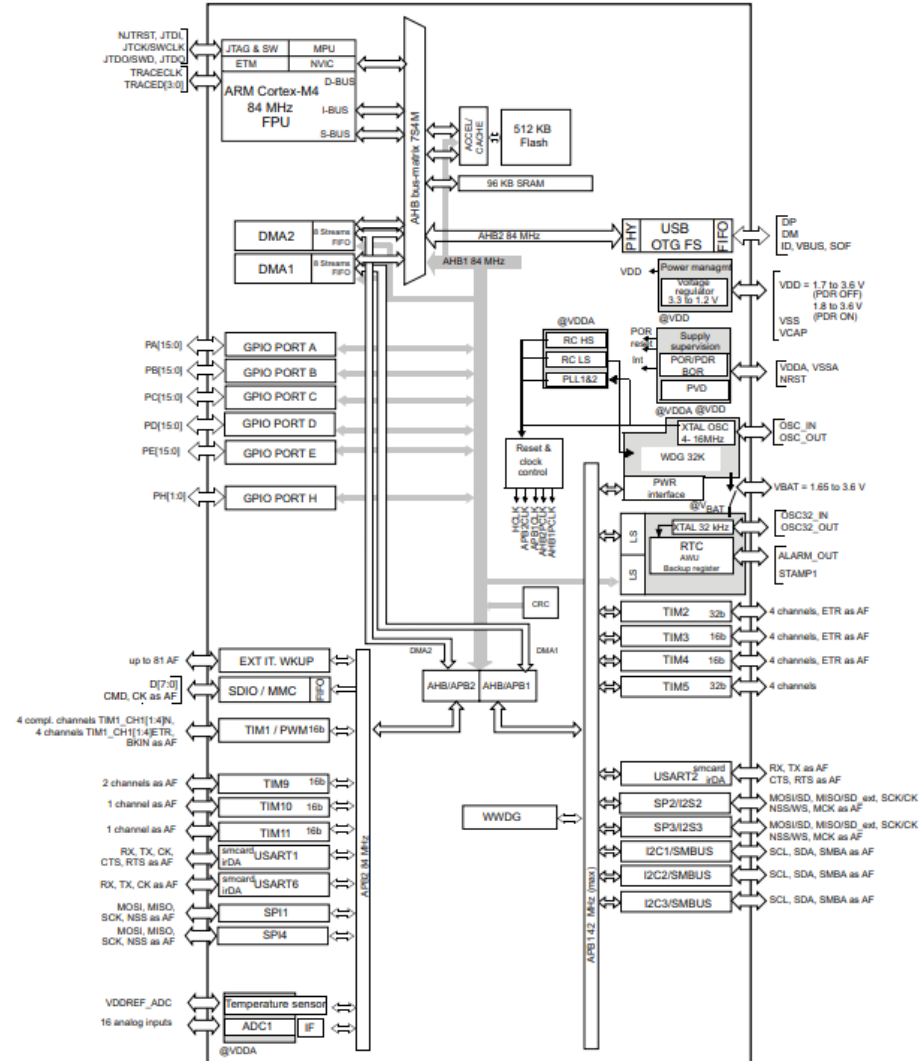
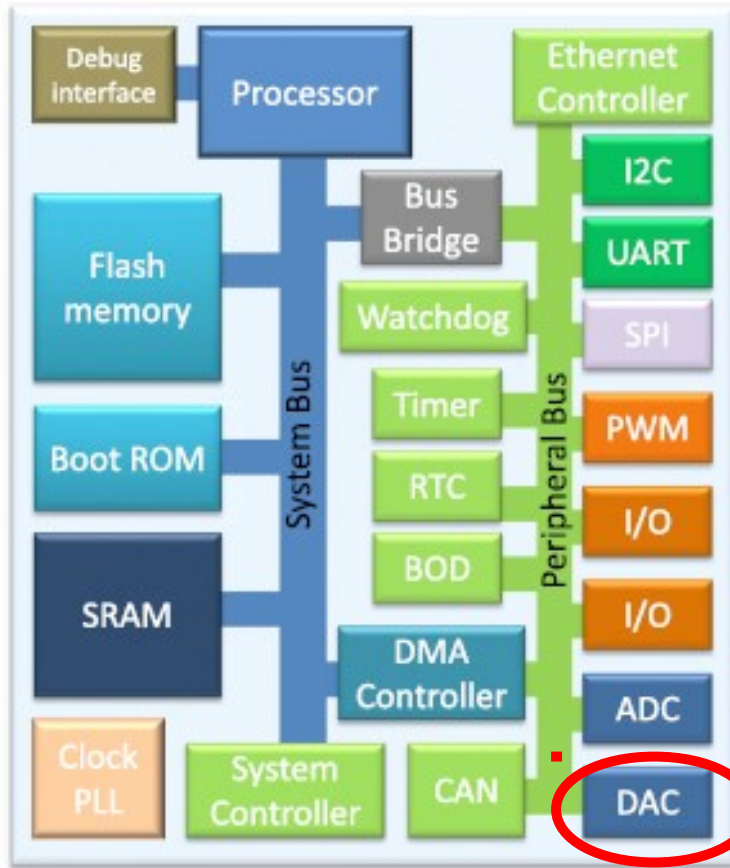




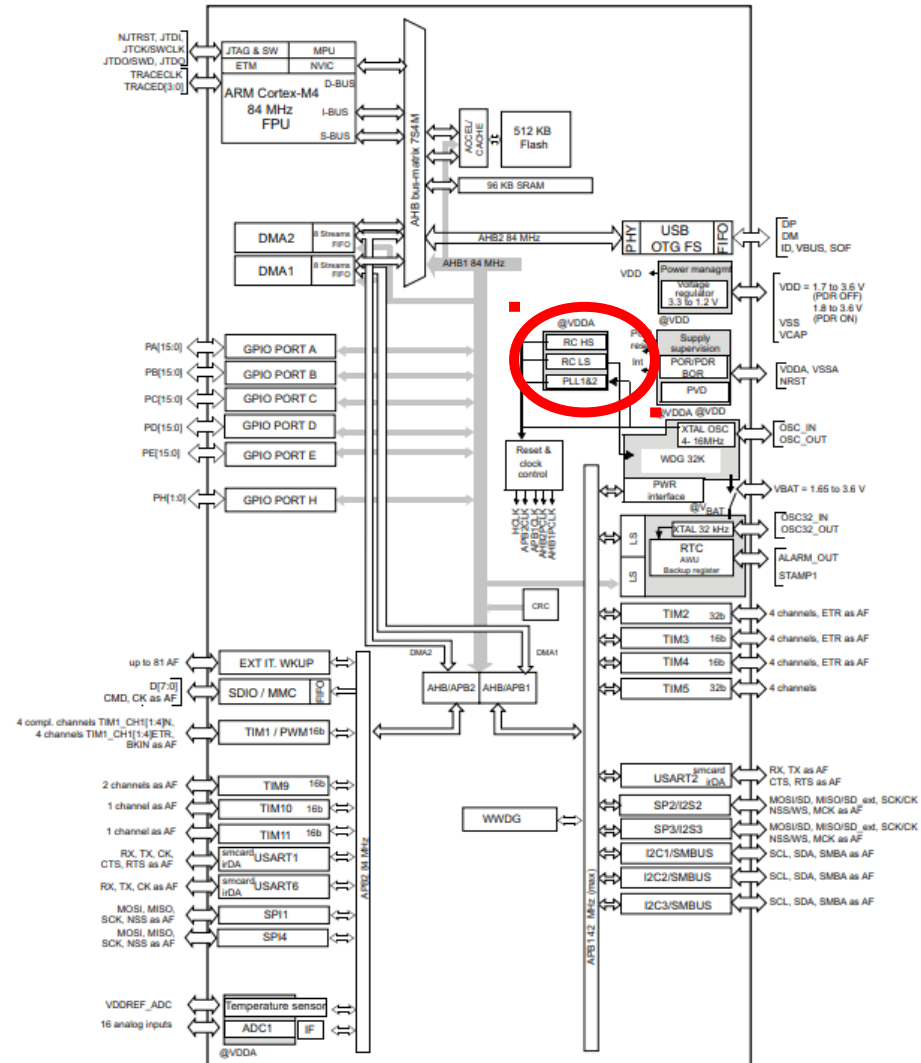
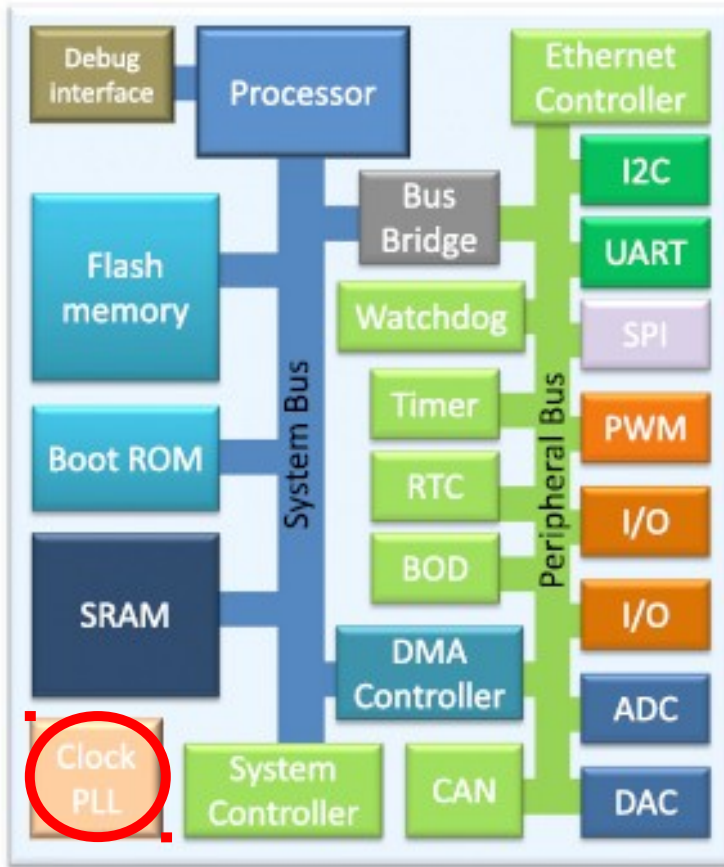
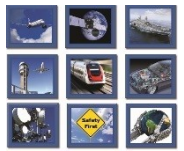
# Architecture



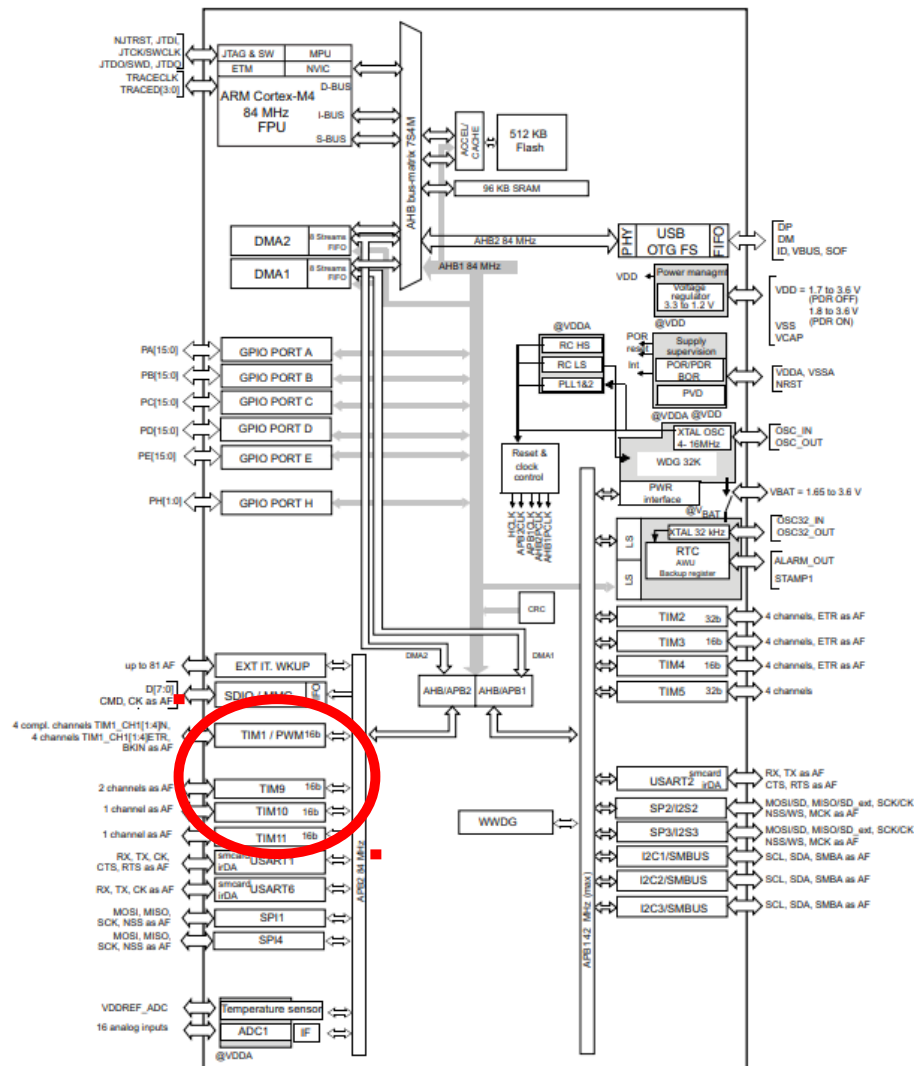
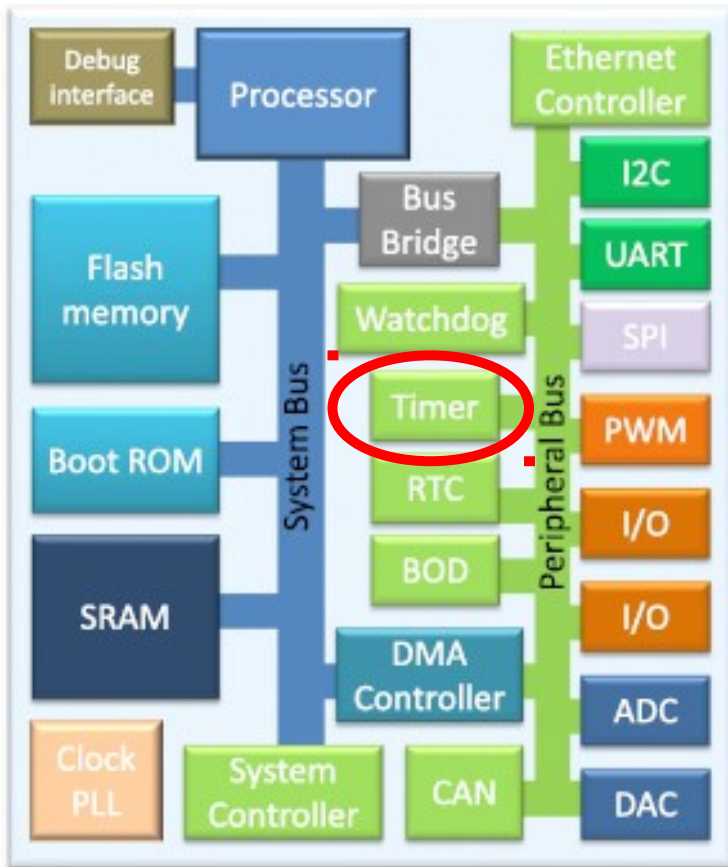
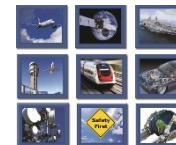
# Architecture



# Architecture

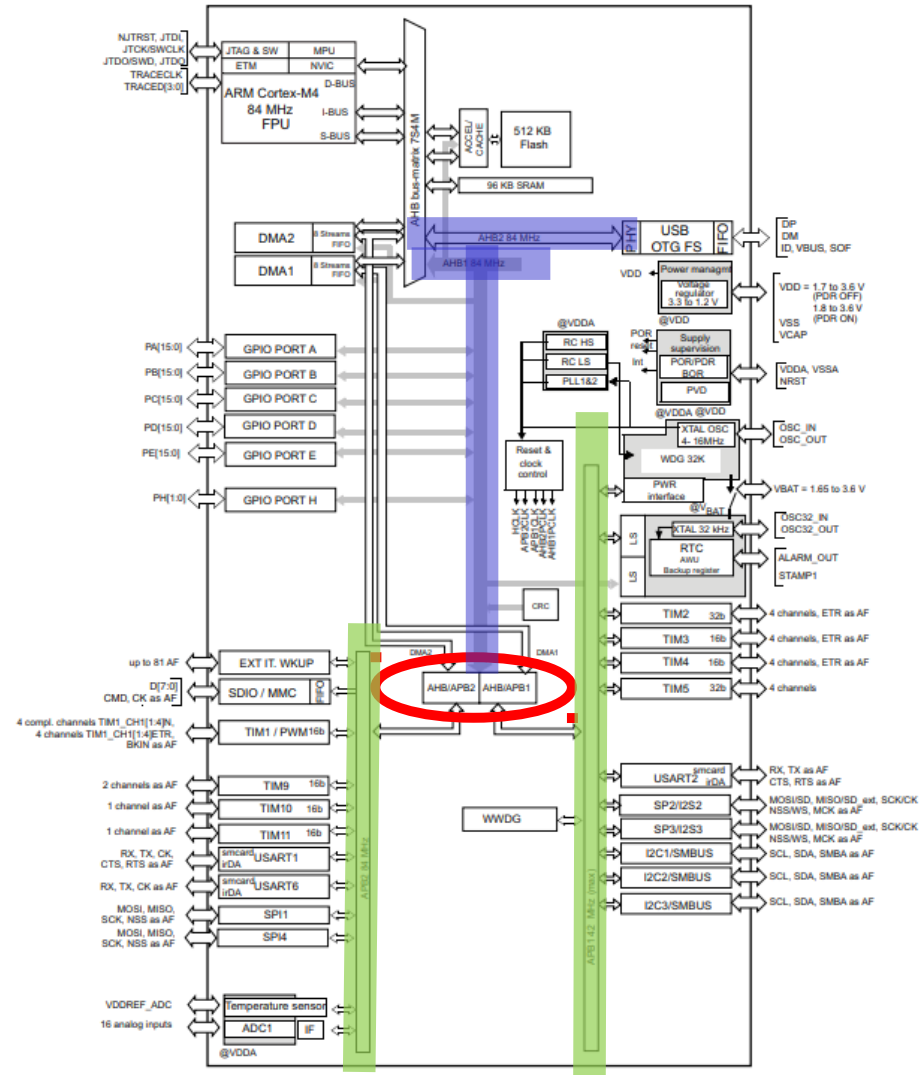
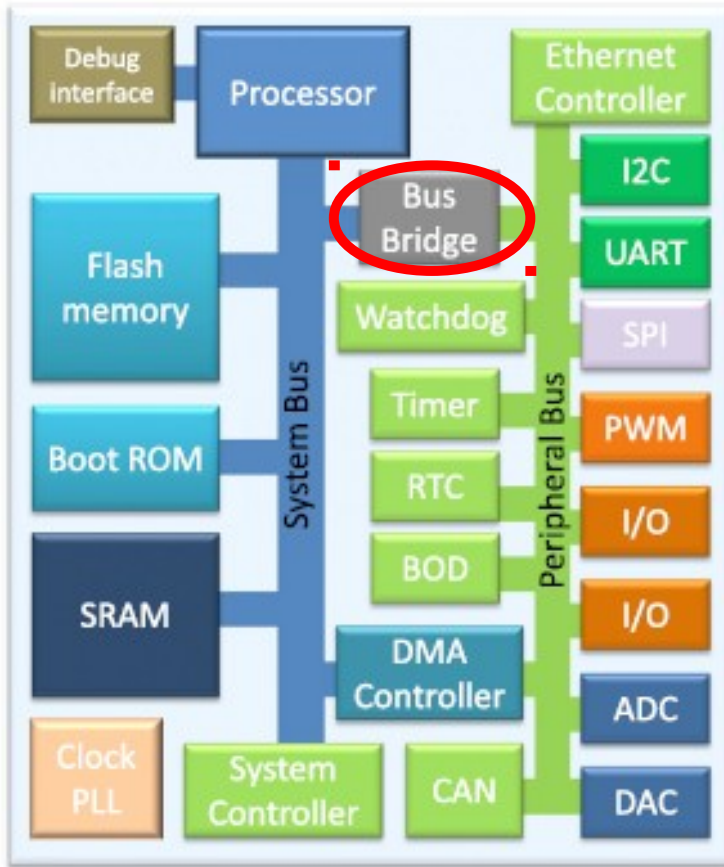


# Architecture

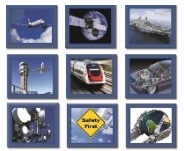




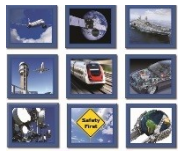
# Architecture





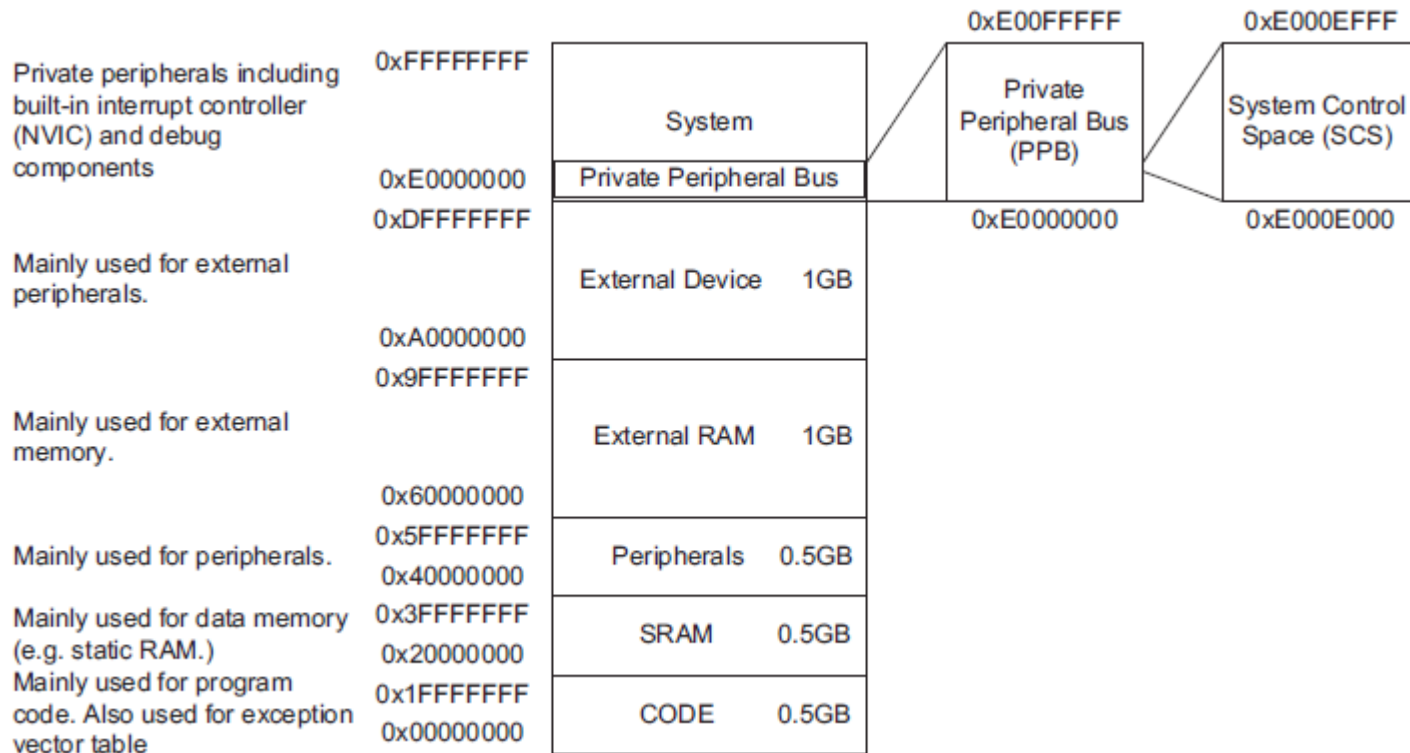


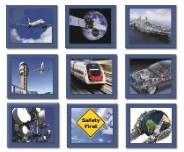
- Cortex M-4
  - Armv7-m architecture: Harvard architecture, 32-bit architecture (internal registers, data path, bus interface)
  - Thumb-2 instruction set (16/32 instructions)
  - Unified memory space 4GB
  - On-chip bus interfaces based on ARM AMBA
  - NVIC controller with priority levels (12 clock cycles)
  - SysTick timer
  - Optimized for power consumption (alternatives: Cortex R or Cortex A)
  - Optional advanced debug features and MPU



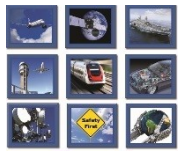
# Cortex M-4

Address space: 4GB, little/big endian





- **Systick Timer**
  - Part of the NVIC, 24-bit decrement timer
  - Sourced from a reference clock source (typ. on-chip)
  - Has its own exception handler
  - Can be used as system clock for an OS (task management, context switch)
  - Used for portability

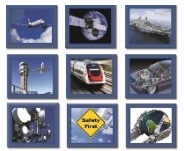


- Power consumption:
  - Various sleep modes available
  - Commands: Wait For Event (WFE) / Wait For Interrupt (WFI)
  - Code stops running
  - Based on the sleep mode, clock signals can selectively be turned off:
    - Deeper sleep mode -> less peripherals running
    - Deeper sleep mode -> higher wakeup time
    - Deeper sleep mode -> less wake-up sources



- **Clock Sources:**
  - External 4-26 Mhz crystal osc. (HSE)
  - Internal 16Mhz factory-trimmed RC (HSI16)
  - Internal 32 Khz low power RC (LSI)
  - External 32 Khz crystal for RTC (LSE)
  - System PLL (uses HSE,HSI16) up to 84Mhz
- At startup, the MCU uses HSI at 16Mhz
- Clock sources managed by Reset and Clock Control (RCC) module





- **Peripherals:**

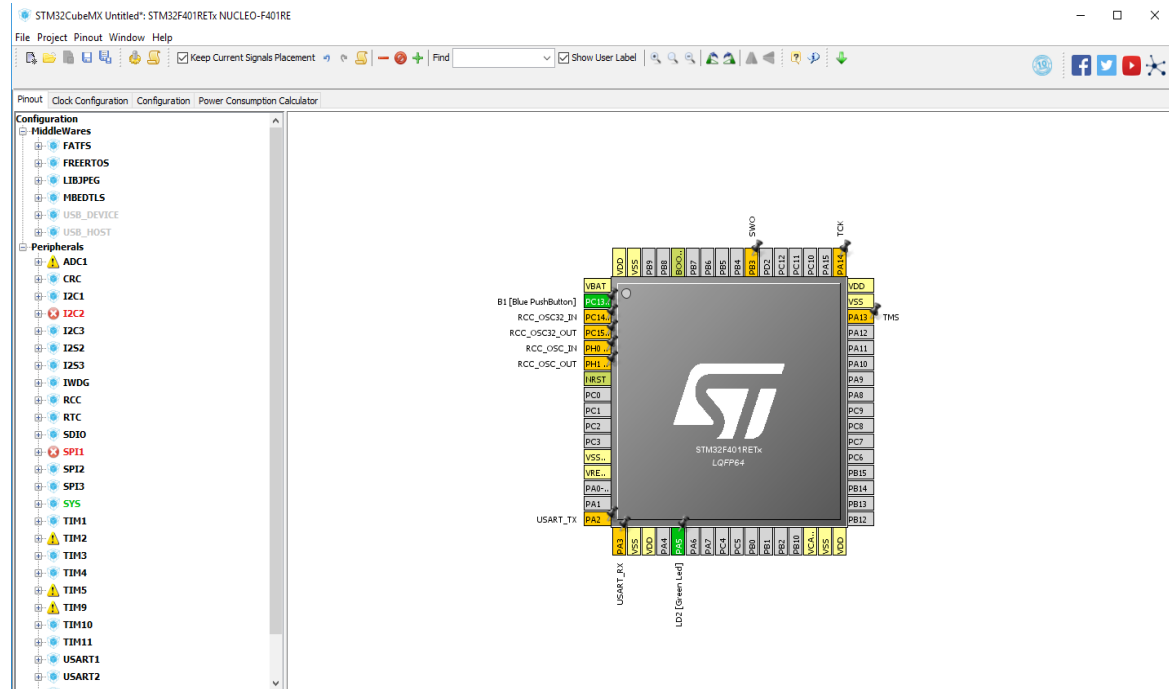
- 11 x Timers
  - 6 x 16bit low power
  - 2 x 32bit
  - 2 x Watchdogs
  - 1 x Systick timer
- 1 x RTC
- 1 x ADC 12 bit
- 2 x SAI Interfaces
- 3 x I2C
- 3 x USART
- 4 x SPI (+ I2S)
- 1 x DMA 16 ch.
- 1 x SDIO
- 1 x USB OTG FS
- 81 x GPIO

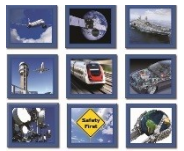


# Getting Started with CubeMX



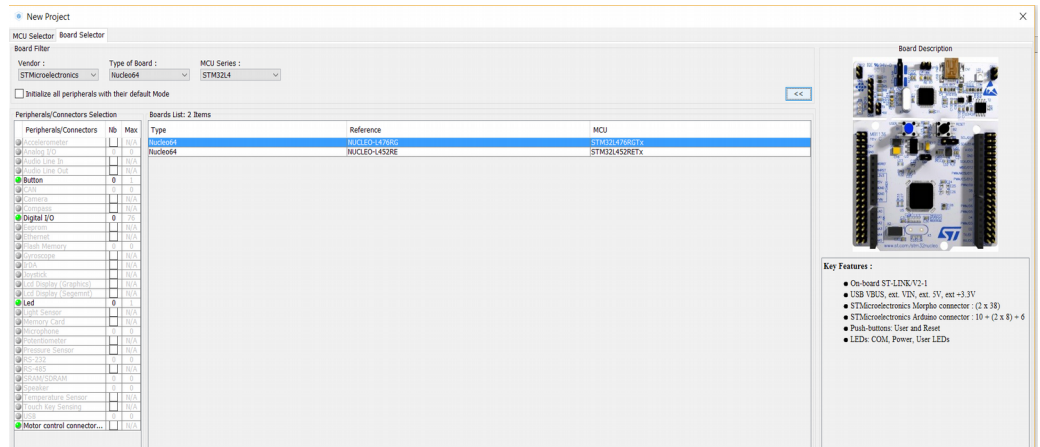
- Configuration tool:
  - Clock sources
  - Peripherals
  - Pinout
  - Middlewares
- Code generation:
  - IDE support





## Usage Example: Clock and Timer 1 configuration

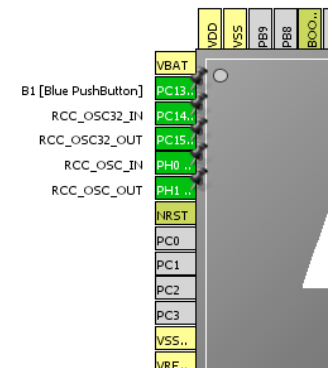
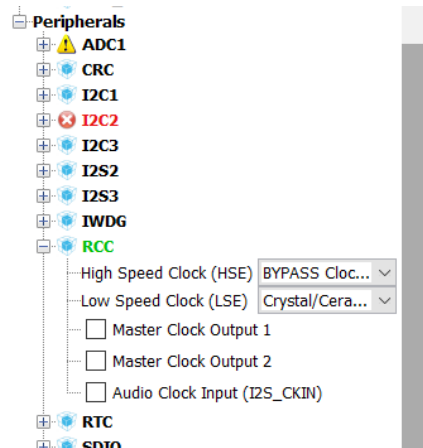
- Step 1:
  - Launch CubeMX
  - Select “New Project”
  - Choose “Board Selector”
  - Vendor “ST Microelectronics”
  - Type of Board “Nucleo 64”
  - MCU Series “Stm32F4”
  - Select “Nucleo-F401RE”
  - Double click on it



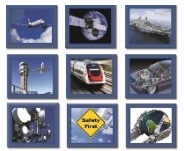


## Usage Example: Clock and LPTimer 1 configuration

- Step 2:
  - From “Pinout” tab
  - Expand “RCC”
  - Select “Crystal/Ceramic resonator” in Low Speed Clock (LSE)
  - This will enable external 32Khz crystal of the Nucleo Board

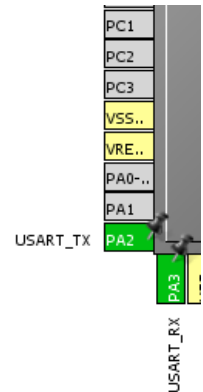
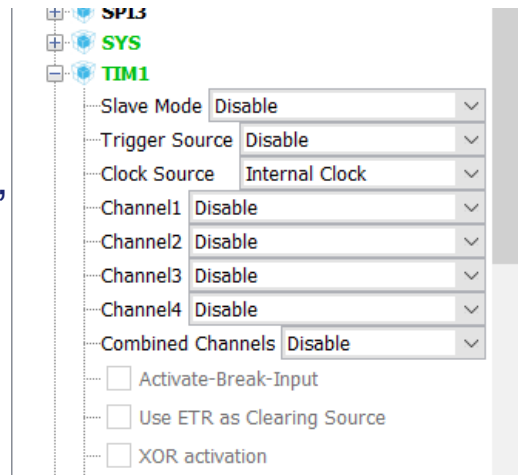






## Usage Example: Clock and Timer 1 configuration

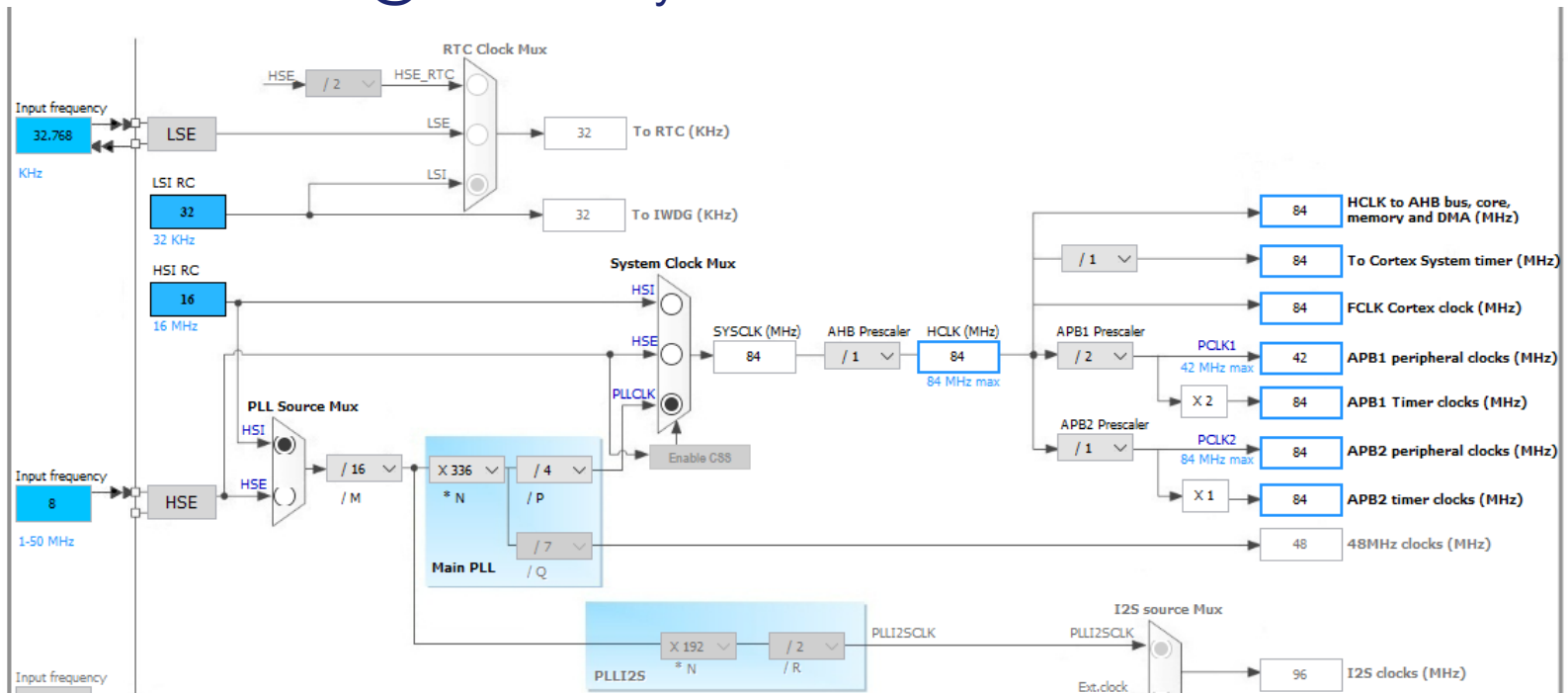
- Step 3:
  - From “Pinout” tab
  - Expand “TIM1”
  - Select “Internal Clock” as clock source





## Usage Example: Clock and Timer 1 configuration

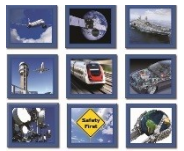
- Step 4:
  - From “Clock Configuration” tab
  - Leave HSI@84Mhz in System Clock Mux





## Usage Example: Clock and Timer 1 configuration

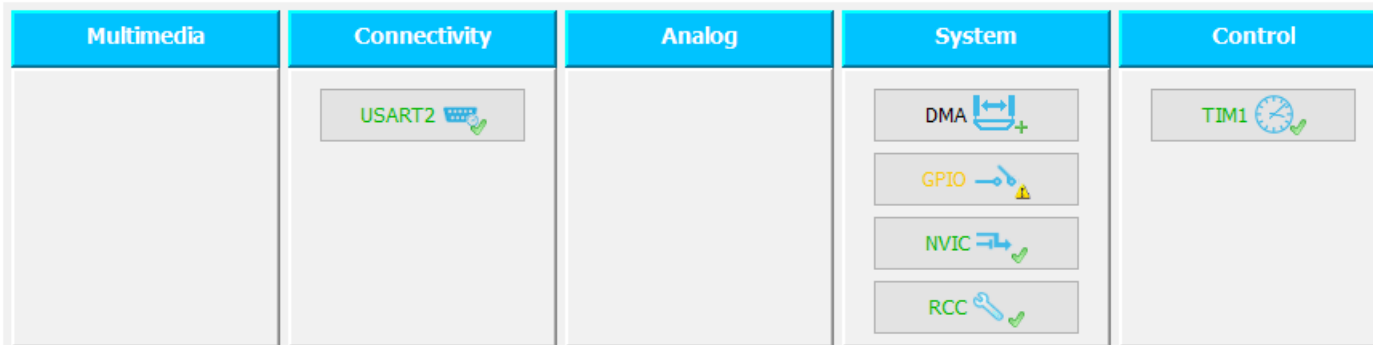
- Step 5:
  - Q: Which bus is connected to TIM1?
  - Annotate its frequency



## Usage Example: Clock and Timer 1 configuration

### Step 7:

- From “Configuration” tab
- Check that peripherals and clocks are set correctly
- Double click on TIM1, select counter period to be 65535
- Q: What prescaler and division should we set for 1ms tick timer?
- NVIC settings enable TIM1 update interrupt





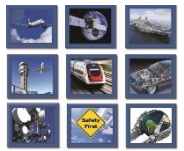
## Usage Example: Code Generation

- Step 1:
  - Click on “Project” -> “Settings”
  - In “Project” tab
  - Set a project name
  - Select SW4STM32 IDE
  - Check that MCU and Firmware package are correct

The screenshot shows the 'Project Settings' dialog box with the 'Project' tab selected. The configuration is as follows:

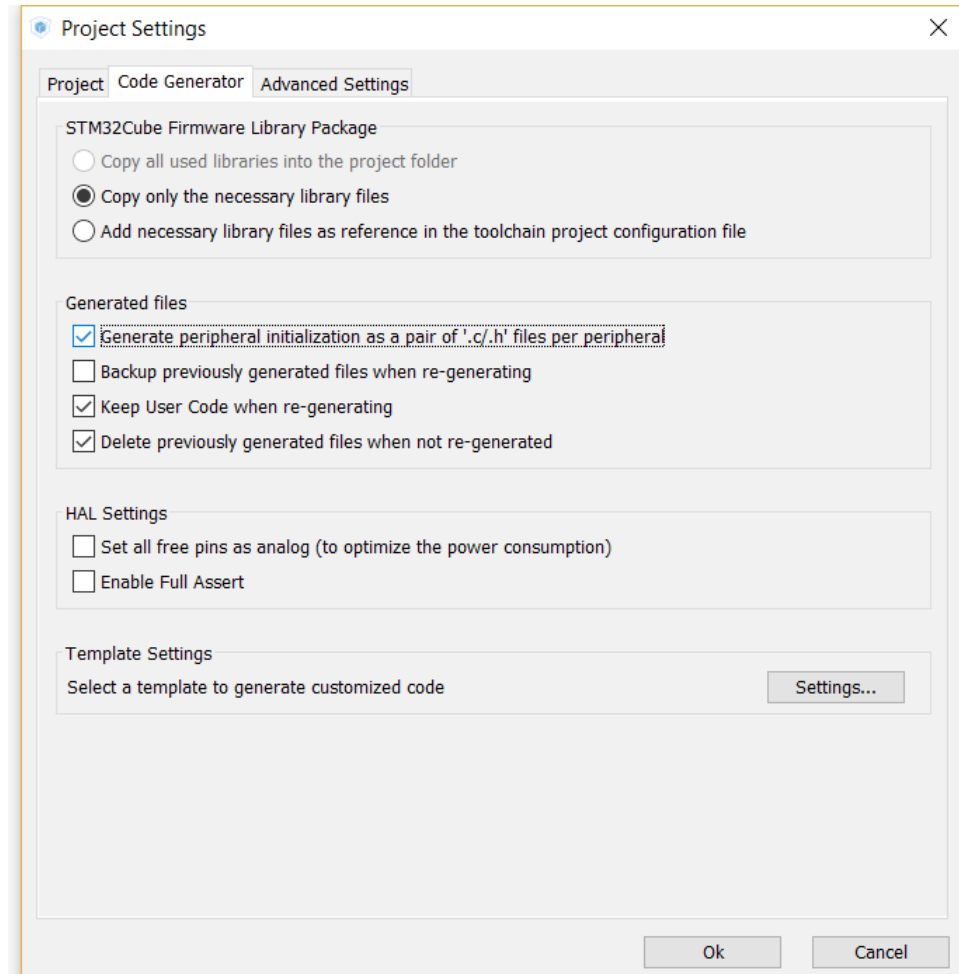
- Project Name:** StartupTest2
- Project Location:** C:\Users\ucole\STMico\Projects
- Toolchain Folder Location:** C:\Users\ucole\STMico\Projects\StartupTest2\
- Toolchain / IDE:** SW4STM32 (selected in a dropdown menu)
- Generate Under Root
- Linker Settings:**
  - Minimum Heap Size: 0x200
  - Minimum Stack Size: 0x400
- Mcu and Firmware Package:**
  - Mcu Reference: STM32F401RETx
  - Firmware Package Name and Version: STM32Cube\_FW\_F4\_V1.19.0
  - Use Default Firmware Location
  - Path: C:/Users/ucole/STM32Cube/Repository/STM32Cube\_FW\_F4\_V1.19.0 (with a 'Browse' button)

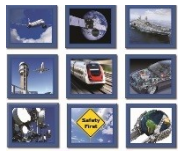
Buttons at the bottom: **Ok** (highlighted with a red dashed box) and **Cancel**.



## Usage Example: Code Generation

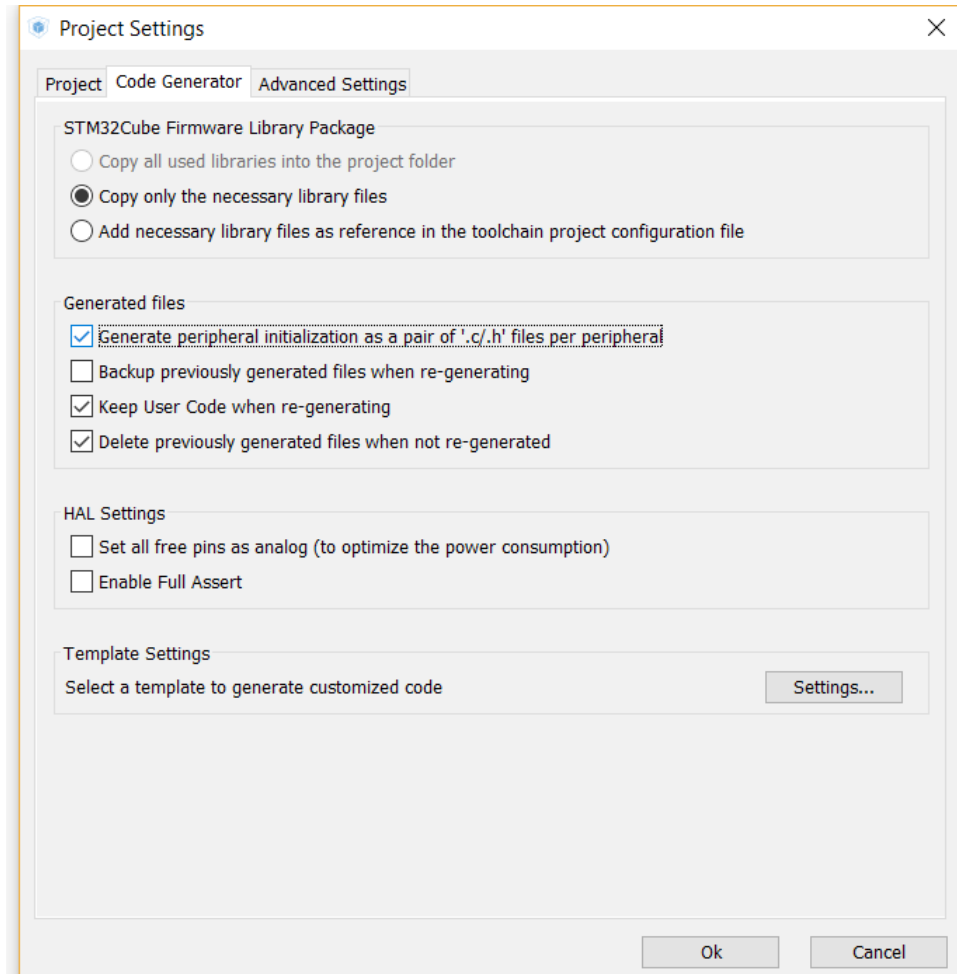
- Step 2:
  - In “Code Generator” tab
  - Select “Generate peripheral initialization...”
  - Keep other options unchanged
  - Click on “OK”



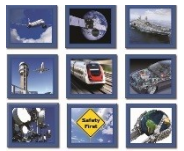


## Usage Example: Code Generation

- Step 3:
  - Click on “Project” -> “Generate Code”
  - Wait the end of the execution
  - You can now import the project on System Workbench 4

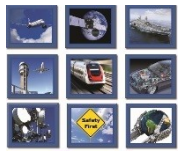






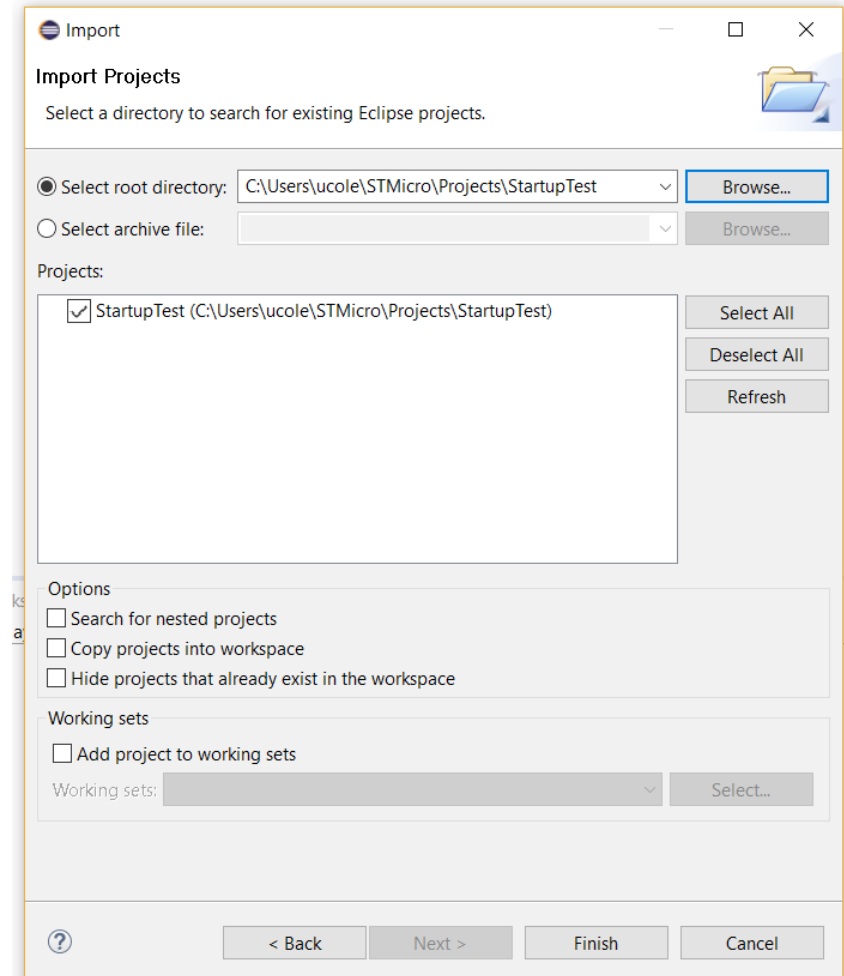
# System Workbench 4

Importing project and debugging



## Importing project generated with CubeMX

- Step 1:
  - Launch SW4STM32
  - In “File” menu click on “import...”
  - In “General”, select “Existing Project into Workspace”
  - Select the root folder generated with CubeMx
  - Keep default options and click finish





## Importing project generated with CubeMX

- Step 2:
  - Right click on the project and select “Build Project”
  - Wait for compilation to finish and check that no errors were generated

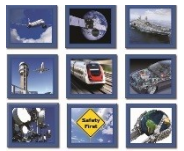


CDT Build Console [StartupTest]

```
Invoking: MCU GCC Linker
arm-none-eabi-gcc -mcpu=cortex-m4 -mthumb -mfloat-abi=hard -mfpu=fpv4-sp-d16 -specs=nosys.specs -specs=nano.specs -T"../STM32L476RGTx_FLASH.ld
Finished building target: StartupTest.elf

C:/Users/ucole/.eclipse/org.eclipse.platform_4.5.2_210783474_win32_win32_x86_64/plugins/fr.ac6.mcu.externaltools.arm-none.win32_1.12.0.2016112
Generating binary and Printing size information:
arm-none-eabi-objcopy -O binary "StartupTest.elf" "StartupTest.bin"
arm-none-eabi-size "StartupTest.elf"
  text    data    bss     dec     hex filename
  6184     24   1624   7832   1e98 StartupTest.elf

19:17:38 Build Finished (took 26s.721ms)
```



## Importing project generated with CubeMX

- Step 3:
  - Plug the nucleo
  - Right click on the project and select “Debug as”
  - When prompted to switch in debug view click yes (check the “keep option” if you don’t want to repeat this step each time)
  - The code will halt on HAL\_Init()
  - Click on “step over” or “step into” to get familiar with the IDE in debugging mode
  - You can click on “Resume” if you want your code to freely run (but it won’t do anything since it’s empty 😊 )



## Important files: the linker script

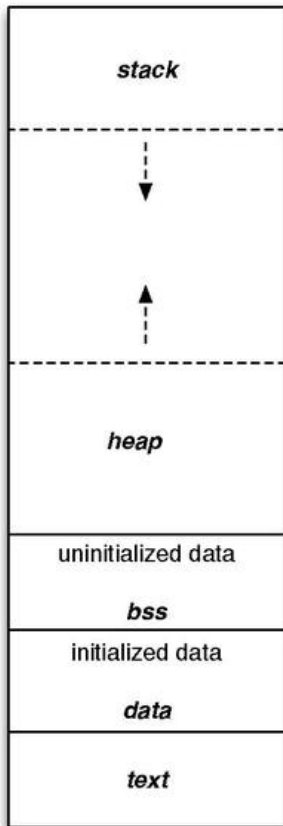
- In project explorer: STM32F401RETx\_FLASH.ld
- Where to find program and data memory (RAM,FLASH) w.r.t. the linear memory map of the MCU
- What to put inside each area (e.g., .isr\_vector, .text and constant data in flash, .data and .bss in ram etc...)

```
32 /* Entry Point */
33 ENTRY(Reset_Handler)
34
35 /* Highest address of the user mode stack */
36 _estack = 0x20018000; /* end of RAM */
37 /* Generate a link error if heap and stack don't fit into RAM */
38 _Min_Heap_Size = 0x200; /* required amount of heap */
39 _Min_Stack_Size = 0x400; /* required amount of stack */
40
41 /* Specify the memory areas */
42 MEMORY
43 {
44 RAM (xrw) : ORIGIN = 0x20000000, LENGTH = 96K
45 FLASH (rx) : ORIGIN = 0x80000000, LENGTH = 512K
46 }
47
48 /* Define output sections */
49 SECTIONS
50 {
51 /* The startup code goes first into FLASH */
52 .isr_vector :
53 {
54 . = ALIGN(4);
55 KEEP(*(.isr_vector)) /* Startup code */
56 . = ALIGN(4);
57 } >FLASH
```



## Important files: the linker script

- Quick recall on memory segments:



Automatic variables,  
returned address ...

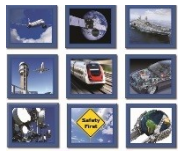
```
int dummy_func(int arg1){
    int arg2;
    if(arg2 > arg1) return arg2;
    else return arg1;
}
```

Dynamic memory allocation (e.g., malloc,...)

Global or static variables initialized to 0 or not explicitly initialized

Global or static variable with pre-defined value and that can be modified

Read only data (e.g., code)

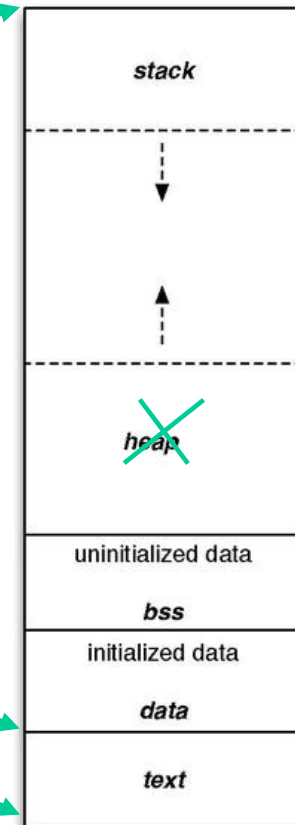


## Important files: the linker script

- Quick recall on memory segments:

```

35 /* Highest address of the user mode stack */
36 _estack = 0x20018000; /* end of RAM */
37 /* Generate a link error if heap and stack don't fit into RAM */
38 _Min_Heap_Size = 0x200; /* required amount of heap */
39 _Min_Stack_Size = 0x400; /* required amount of stack */
40
41 /* Specify the memory areas */
42 MEMORY
43 {
44 RAM (xrw) : ORIGIN = 0x20000000, LENGTH = 96K
45 FLASH (rx) : ORIGIN = 0x80000000, LENGTH = 512K
46 }
    
```

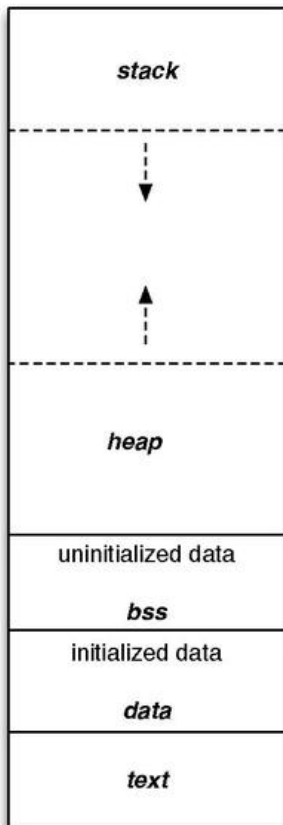






## Important files: the linker script

- Quick recall on memory segments:



```

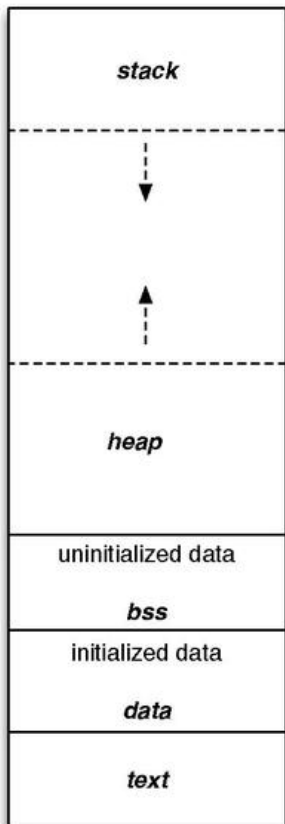
18 /* Define output sections */
19 SECTIONS
20 {
21 /* The startup code goes first into FLASH */
22 .isr_vector :
23 {
24     . = ALIGN(8);
25     KEEP(*(.isr_vector)) /* Startup code */
26     . = ALIGN(8);
27 } >FLASH
28
29 /* The program code and other data goes into FLASH */
30 .text :
31 {
32     . = ALIGN(8);
33     *(.text)           /* .text sections (code) */
34     *(.text*)          /* .text* sections (code) */
35     *(.glue_7)         /* glue arm to thumb code */
36     *(.glue_7t)        /* glue thumb to arm code */
37     *(.eh_frame)
38
39     KEEP (*(.init))
40     KEEP (*(.fini))
41
42     . = ALIGN(8);
43     _etext = .;        /* define a global symbols at end of code */
44 } >FLASH
45
46 /* Constant data goes into FLASH */
47 .rodata :
48 {
49     . = ALIGN(8);
50     *(.rodata)         /* .rodata sections (constants, strings, etc.) */
51     *(.rodata*)        /* .rodata* sections (constants, strings, etc.) */
52     . = ALIGN(8);
53 } >FLASH
54

```



## Important files: the linker script

- Quick recall on memory segments:



```

/* used by the startup to initialize data */
_sidata = LOADADDR(.data);

/* Initialized data sections goes into RAM, load LMA copy after code */
.data :
{
    . = ALIGN(8);
    _sidata = .;          /* create a global symbol at data start */
    *(.data)             /* .data sections */
    *(.data*)           /* .data* sections */

    . = ALIGN(8);
    _edata = .;         /* define a global symbol at data end */
} >RAM AT> FLASH

/* Uninitialized data section */
. = ALIGN(4);
.bss :
{
    /* This is used by the startup in order to initialize the .bss section */
    _sbss = .;          /* define a global symbol at bss start */
    __bss_start__ = _sbss;
    *(.bss)
    *(.bss*)
    *(COMMON)

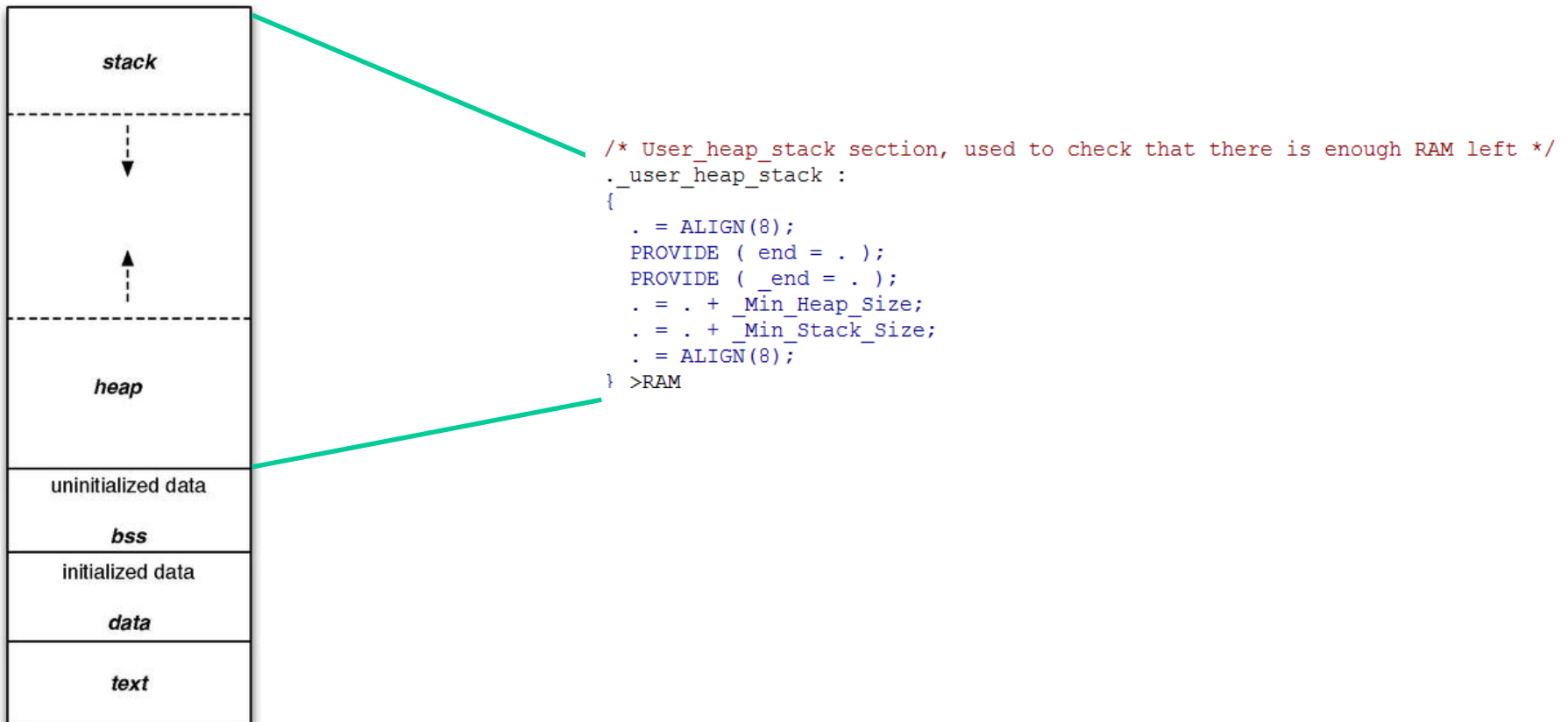
    . = ALIGN(4);
    _ebss = .;          /* define a global symbol at bss end */
    __bss_end__ = _ebss;
} >RAM

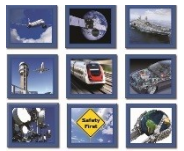
```



## Important files: the linker script

- Quick recall on memory segments:





## Important files: the startup file

- startup/startup\_stm32f401xe.s
- Written in assembly, it holds the reset handler (first code to be executed) and the vector table

```
76
77     .section    .text.Reset_Handler
78     .weak      Reset_Handler
79     .type       Reset_Handler, %function
80 Reset_Handler:
81     ldr        sp, =_estack    /* Atollic update: set stack pointer */
82
83 /* Copy the data segment initializers from flash to SRAM */
84     movs      r1, #0
85     b         LoopCopyDataInit
86
87 CopyDataInit:
88     ldr        r3, =_sidata
89     ldr        r3, [r3, r1]
90     str        r3, [r0, r1]
91     adds      r1, r1, #4
92
93 LoopCopyDataInit:
94     ldr        r0, =_sdata
95     ldr        r3, =_edata
96     adds      r2, r0, r1
97     cmp       r2, r3
98     bge       CopyDataInit
```



## Important files: the system file

- Src/system\_stm32f4xx.c
- SystemInit function for clock and vector table initialization
- Other clock utilities...

```
main.c startup_stm32f4/6x... stm32f4xx_hal.c stm32f4xx_hal_msp.c STM32L476RGTX_FLASH... system_stm32f4xx.c
198 void SystemInit(void)
199 {
200     /* FPU settings -----*/
201     #if ( __FPU_PRESENT == 1) && ( __FPU_USED == 1)
202         SCB->CPACR |= ((3UL << 10*2)| (3UL << 11*2)); /* set CP10 and CP11 Full Access */
203     #endif
204     /* Reset the RCC clock configuration to the default reset state -----*/
205     /* Set MSION bit */
206     RCC->CR |= RCC_CR_MSION;
207
208     /* Reset CFGR register */
209     RCC->CFGR = 0x00000000;
210
211     /* Reset HSEON, CSSON , HSION, and PLLON bits */
212     RCC->CR &= (uint32_t)0xEAF6FFFF;
213
214     /* Reset PLLCFGR register */
215     RCC->PLLCFGR = 0x00001000;
216
217     /* Reset HSEBYP bit */
218     RCC->CR &= (uint32_t)0xFFFFBFFF;
219
220     /* Disable all interrupts */
221     RCC->CIER = 0x00000000;
222
223     /* Configure the Vector Table location add offset address -----*/
224     #ifdef VECT_TAB_SRAM
225         SCB->VTOR = SRAM_BASE | VECT_TAB_OFFSET; /* Vector Table Relocation in Internal SRAM */
226     #else
227         SCB->VTOR = FLASH_BASE | VECT_TAB_OFFSET; /* Vector Table Relocation in Internal FLASH */
228     #endif
229 }
```





# Thank You!

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